High-Speed Bi-directional Digital I/O Board for PCI Express



* Specifications, color and design of the products are subject to change without notice.

Features

 32channels of unisolated LVTTL level I/O (32 input channels / each 16channels for I/O / 32 output channels are selected.)

This product has the 32channels (operating voltage 3.3VDC, positive logic) of unisolated LVTTL level I/O whose response speed is 20nsec. They can be used for 32bit input, 16bit input plus 16bit output, or for 32bit output.

Other than I/O bit, this product has the control signal (clock, start, stop and handshake signal (REQ, ACK) that can control starting and stopping the sampling (input) / generating (output)).

Sampling and generating with transfer rate at 50MHz maximum

Bus master transfer makes it possible to sample (input) or generate (output) large data with transfer rate at 50MHz maximum. As the sampling and generating features have their own bus mastering blocks each made up of two independent channels, the board can generate 16 signals while sampling 16 signals.

 A synchronization control connector is provided for synchronized control of multiple boards.

A synchronization control connector is provided for synchronized control of up to 16 boards. It is also easy to synchronize operation with other CONTEC boards that have a synchronization control connector.

- You can use Max. 4 input signals as interrupt request signals at the time of using the general-purpose I/O.

You can use Max. 4 input signals as interrupt request signals and also disable or enable the interrupt in bit units at the time of using the general-purpose I/O.

- Windows compatible driver libraries are attached.

Using the attached driver library API-PAC(W32) makes it possible to create applications of Windows. In addition, a diagnostic program by which the operations of hardware can be checked is provided.

- You can use pull-up and the voltage selection.

At input points and control signals, you can use pull-up. In addition, the pull-up voltage can be selected from the 3.3V and 5V. This feature allows you to easily connect and equipment with an output point of the sink type.

 Functions and connectors are compatible with PCI compatible board PIO-32DM(PCI) and PCI Express compatible board DIO-32DM2-PE, DIO-32DM-PE.

The functions same with PCI compatible board PIO-32DM(PCI) and PCI Express compatible board DIO-32DM2-PE, DIO-32DM-PE are provided. In addition, as there is compatibility in terms of connector shape and

This product is a PCI Express bus-compliant interface board that supports transfer by bus mastering and performs input/output between the external device and digital signal. This product features unisolated LVTTL level (Operating voltage: 3.3V) I/O 32channels and you can select input / output in 16 units.

Bus master transfer makes it possible to sample quickly large data with transfer rate at 50MHz maximum. It can be used as a pattern generator that outputs arbitrary digital patterns at high speed. It can also be used as a general-purpose I/O board when bus mastering is not used.

Windows driver is bundled with this product.

Using the dedicated library VI-DAQ makes it possible to create each application for LabVIEW.

- * The contents in this document are subject to change without notice.
- * Visit the CONTEC website to check the latest details in the document.
- * The information in the data sheets is as of September, 2018.

pin assignments, it is easy to migrate from the existing system.

LabVIEW is supported by a plug-in of dedicated library.
 Using the dedicated library makes it possible to make a LabVIEW application.

Specification

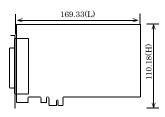
Item	Specifications
Digital section	•
Number of I/O Channels	32channels (select input 32channels / I/O each 16channels / output 32 channels by software)
I/O circuit	· , ,
Operating voltage	3.3VDC
Built-in power	None
Input section	
Input format	Unisolated LVTTL level (Equivalent to 74LVT245B) (positive logic) * 5VTTL level input enabled
Pull-up	None/3.3V/5V
Interrupt	<when general-purpose="" i="" is="" o="" used=""> 4 interrupt input signals are arranged into a single output of interrupt signal INTA An interrupt is generated at the rising edge (LOW-to-HIGH transition).</when>
Pull-up resistor	10kΩ
Output section	
Output format	Unisolated LVTTL level (Equivalent to 74LVT245B) (positive logic)
Rating (Max.)	3.3VDC 32mA
Response time	20nsec
Data access method	General-purpose digital I/O or I/O with bus master transfer
Echo-back function	Available (at general-purpose output)
Pattern input	
Sampling start trigger	Software start/External start/Pattern match/SC connector
Sampling stop trigger	Software stop/External stop/End of transfer/Transfer error/Specified number of items/SC connector
Sampling clock	Sampling timer/External clock input/handshake/SC connector
Sampling timer	20ns - 21s, 5ns unit
Pattern output	
Generating start trigger	Software start/External start/SC connector
Generating stop trigger	Software stop/External stop/End of transfer/Transfer error/Specified number of items/SC connector
Generating clock	Output timer/External clock input/Handshake/SC connector
Generating timer	20ns - 21s, 5ns unit
Control signal	
I/O signal level	Unisolated LVTTL level *5VTTL level input enabled , *3.3V / 5V pull-up can be set
REQ signal (handshake)	Negative logic tL=25ns (Min.)
ACK signal (handshake)	Negative logic tL=25ns (Min.)
External start signal	Selection of rising/falling edge with the software
External stop signal	Selection of rising/falling edge with the software
External clock input	f=20 MHz (Max.)

DIO-32DM3-PE



Item	Specifications				
Bus master section					
DMA channels	2channels (one each for input and output)				
Transfer bus width	64/32bit width				
Transfer rate	360 MB/sec.				
FIFO	4K data/ch.				
Scatter/Gather function	2GB/ch.				
Synchronization section					
Control output signal	Selection of output signal with the software when specifying a sync master board.				
Control input signal	Selection of sync factor with the software when specifying sync slave boards.				
Max. board count for connection	16 boards including the master board				
Common section					
Allowable distance of signal extension	1.5m (dependent on wiring environment)				
Memory addresses	Occupies 2 locations 256MByte				
Current consumption	3.3V 600mA (Max.) , 12V 30mA (Max.)				
Operating conditions	0 - 50°C, 10 - 90%RH (No condensation)				
Bus specification	PCI Express Base Specification Rev.2.0 x1				
Physical dimensions (mm)	169.33(L) x 110.18(H)				
Connector	PCR-E96LMD+equivalence to it [mfd. by HONDA TSUSHIN KOGYO CO., LTD.]				
Weight	150g				
Standard	VCCI Class A, FCC Class A, CE Marking (EMC Directive Class A, RoHS Directive)				

External Board Dimensions



[mm]

The standard outside dimensions (L) is the distance from the end of the board to the outer surface of the slot cover.

Differences in Bus Master Transfer Rate by System Configuration

When Fitted in the PC Expansion Slot

	Lim	Limited		nited	
	In	Out	In	Out	
Core i5-4590 3.30GHz	50	50	22.2	8.3	
Core i5-6600 3.30GHz	50	50	25	11.7	
Core i7-2600K 3.40GHz	50	50	15.3	7.1	
11 11 15 14 1 2					

Unit [MHz]

When CONTEC's Expansion Unit ECH-PE-CE Series Is Used

	Lim	ited	Unlimited		
	In	Out	In	Out	
Core i5-4590 3.30GHz	50	50	11.1	1.8	
Core i5-6600 3.30GHz	50	50	13.3	6.0	
Core i7-2600K 3.40GHz	50	50	12.5	5.0	

Unit [MHz]

Packing List

Product [DIO-32DM3-PE] ...1

SC Cable (10cm) ...1

Disk *1 [API-PAC(W32)] ...1

First step guide ... 1

Warranty Certificate ...1

Serial Number Label ...1

Support Software

Windows version of digital I/O driver API-DIO(WDM)

[Stored on the bundled disk driver library API-PAC(W32)]

The API-DIO(WDM) is the Windows version driver library software that provides products in the form of Win32 API functions (DLL). Various sample programs such as Visual Basic and Visual C++, etc and diagnostic program *1useful for checking operation is provided.

For more details on the supported OS, applicable language and new information, please visit the CONTEC's Web site.

LabVIEW-support data acquisition library DAQfast for LabVIEW (Available for downloading (free of charge) from the CONTEC web

This is a data collection library to use in the LabVIEW by National Instruments. With Polymorphic VI, our design enables a LabVIEW user to operate seamlessly. Our aim is that the customers to perform easily, promptly what they wish to do.

For more details on the library and download of DAQfast for LabVIEW, please visit the CONTEC's Web site.

Data acquisition library for LabVIEW VI-DAQ

(Available for downloading (free of charge) from the CONTEC web

This is a VI library to use in National Instruments LabVIEW. VI-DAQ is created with a function form similar to that of LabVIEW's Data Acquisition VI, allowing you to use various devices without complicated settings.

For more details on the library and download of VI-DAQ, please visit the CONTEC's Web site.

List of Options

Shield Cable with 96-Pin Half-Pitch Connectors at Both Ends

PCB96PS-0.5P (0.5m)

PCB96PS-1.5P (1.5m)

Shield Cable with 96-Pin D-SUB Connector at One End

PCA96PS-0.5P (0.5m)

PCA96PS-1.5P (1.5m)

Accessories (Option)

Screw Terminal Unit (M3 x 96P)

EPD-96A *1*2

Screw Terminal Unit (M3.5 x 96P)

EPD-96 *1

Terminal Unit for Cables (M3 x 96P)

DTP-64A *1

■ DIO-32DM3-PE ■

[&]quot;Limited" indicates that the number of transfers is designated and "unlimited" indicates the number of transfers is not designated. However, these values may not be satisfied depending on the system configuration, such as other boards and applications.

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^{*1} The bundled disk contains the driver software and User's Guide

PCB96P or PCB96PS optional cable is required separately.

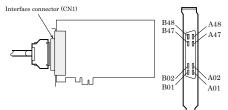
^{*2 &}quot;Spring-up" type terminal is used to prevent terminal screws from falling off.

^{*} Check the CONTEC's Web site for more information on these options.

How to connect the connectors

Connector shape

To connect an external device to this product, plug the cable from the device into the interface connector (CN1) shown below.



- Connector used Connector used PCR-E96LMD+ [mfd. by HONDA TSUSHIN KOGYO CO., LTD.]
- ROGYO CO., LTD.]

 or equivalence to it
 Compatible connectors
 PCR-E96FA+
 [mfd. by HONDA TSUSHIN
 KOGYO CO., LTD.] or equivalence to it
- * Please refer to chapter 1 for more information on the supported cable and accessories.

GND B48 GND B47 GND B46 EXTCLK1 B45 GND B44 EXTSTART1 B43 GND B42 EXTSTOP1 B41 GND B40 EXTREQ1 B39 GND B38 EXTREQ1 B39 GND B38 EXTREQ1 B39 GND B38 EXTREQ1 B39 GND B38 EXTREQ1 B39 GND B35 GND B35 GND B35 GND B35 GND B36 GND B37 GND B38 DIODO06 B31 GND B32 DIODO06 B31 GND B32 DIODO08 B29 GND B28 DIODO08 B29 GND B26 DIODO08 B27 GND B27 GND B28 DIODO08 B29 GND B28 DIODO08 B29 GND B29 GND B20 GND B20 DIODO08 B21 GND B21 DIOCO08 B15 GND B10 DIOCO08 B10 GND B10 DIOCO08 B10 GND B00 DIOCO08 B10 GND B00 DIOCO08 B00 DIOCO01 B05 GND B00 DIOCO01 B05 DIO	Connector Pin Assig	nment					
GND B46 EXTCLK1 B45 GND B44 EXTSTART1 B43 GND B42 EXTSTOP1 B41 GND B42 EXTSTOP2 B41 GND B39 GND B39 GND B38 EXTACK1 B37 GND B36 GND B35 GND B35 GND B35 GND B35 GND B35 GND B36 GND B35 GND B35 GND B36 GND B37 GND B36 GND B37 GND B38 DIDDOOS B39 GND B30 DIDDOOS B29 GND B30 GND B30 DIDDOOS B29 GND B22 DIDDOOS B29 GND B22 DIDDOOS B27 GND B24 DIDDOOS B27 GND B26 DIDDOOS B27 GND B27 GND B28 DIDDOOS B29 GND B20 GND B20 DIDDOOS B27 GND B20 A22 GND A23 DIDOOS A25 DIDOOS A26 GND A27 DIDOOS A27 DIDOOS A28 GND A29 DIDOOS A29 DIDOOS A29 DIDOOS A29 DIDOOS A21 DIDOOS A22 GND A21 DIDOOS A23 DIDOOS A22 GND A24 GND A25 DIDOOS A25 DIDOOS A26 GND A27 DIDOOS A27 DIDOOS A28 GND A29 DIDOOS A20 GND A21 DIDOOS A21 DIDOOS A25 DIDOOS A26 GND A27 DIDOOS A27 DIDOOS A28 GND A28 GND A29 DIDOOS A29 DI	GND I	B48				A48	GND
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SHIND B40 SAND B40	GND I	B42			\neg	A42	GND
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DIODO1 B21 A21 DIOB01 A20 GND	DIOD02 I	B23				A23	
A20 GND B20 A20 GND A19 DiDB00 A19 DiDB00 A18 GND B18 A17 DiDA07 A16 GND A15 DiDA06 A15 DiDA06 A15 DiDA06 A15 DiDA06 A15 DiDA06 A16 GND A16 GND A17 DiDA07 A16 GND A17 DiDA06 A17 DiDA06 A17 DiDA06 A17 DiDA06 A17 DiDA06 A18 DiDA06 A19 DiDA06 A19 DiDA06 A10 DiDA05 A11 DiDA04 A10 GND A10 GND A10 GND A10 GND A09 DiDA03 * A08 GND A08 GND A07 DiDA02 * A06 GND A07 DiDA01 * A07 DID	GND I	B22				A22	GND
DIOCOO B19 A19 DIOBOO	DIOD01	B21				A21	DIOB01
SND B18 DIOCO7 B17 A17 DIOA07 A16 GND A15 DIOCO6 B15 A15 DIOA06 A15 DIOA06 A14 GND A15 DIOA06 A14 GND A15 DIOA05 A15 DIOA05 A15 DIOA05 A15 DIOA05 A16 GND A17 DIOA05 A17 DIOA05 A18 DIOA05 A19 DIOA05 A19 DIOA05 A19 DIOA05 A19 DIOA04 A10 GND A09 DIOA03* A09 DIOA03* A09 DIOA03* A09 DIOA03* A09 DIOA03* A07 DIOA02* A07 DIOA02* A07 DIOA01*	GND I	B20				A20	GND
DIOCO7 B17 S17 S18	DIOD00 I	B19				A19	DIOB00
GND B16 DIOCO6 B15 GND B14 DIOCO5 B13 GND B12 DIOCO4 B11 GND B10 DIOCO5 B13 GND B10 DIOCO3 B09 GND B08 DIOCO2 B07 GND B06 DIOCO1 B05 GND B06 DIOCO1 B05 GND B04 A16 GND A17 DIOA06 A14 GND A13 DIOA05 A12 GND A11 DIOA04 A10 GND A09 DIOA03* A09 DIOA03* A08 GND A07 DIOA02* A06 GND A07 DIOA01* A07 DIOA01* A08 GND A07 DIOA01* A08 GND A07 DIOA01*	GND I	B18				A18	GND
DIOC06 B15 A15 DIOA06 A14 GND A15 DIOA06 A14 GND A15 DIOA05 A12 GND A12 GND A12 GND A12 GND A12 GND A11 DIOA04 A11 DIOA04 A10 GND A10 GND A10 GND A10 GND A11 DIOA04 A10 GND A11 DIOA04 A10 GND A11 DIOA04 A10 GND A11 DIOA04 A10 GND A07 DIOA03* A08 GND A07 DIOA02* A07 DIOA02* A07 DIOA02* A08 GND A07 DIOA01* A08 DIOA	DIOC07 I	B17				A17	DIOA07
GND B14 DIOC05 B13 GND B12 A13 DIOA05 A12 GND A11 DIOA05 A12 GND B12 A11 DIOA04 A11 DIOA04 A11 DIOA04 A10 GND B08 DIOC03 B09 GND B08 DIOC02 B07 GND B06 DIOC01 B05 GND B04 A06 GND A07 DIOA02* A07 DIOA01* A08 GND A08 GND A09 DIOA01* A09 DIOA01* A07 DIOA01* A08 GND A09 DIOA01* A09 DIOA01* A07 DIOA01* A07 DIOA01* A07 DIOA01* A08 GND A08 GND A09 DIOA01* A09 DIOA01* A07 DIOA01* A08 DIOA01* A08 DIOA01* A09 DIOA01* A	GND I	B16				A16	GND
GND B14 DIOC05 B13 GND B12 DIOC04 B11 GND B10 DIOC03 B09 GND B08 DIOC02 B07 GND B06 DIOC01 B05 GND B06 DIOC01 B05 GND B04 A07 DIOC02 B07 A08 GND B08 A07 DIOC01 B05 GND B04 A08 GND A07 A08 GND A07 A08 GND A08 A08 GND A07 A08 A08 A08 A08 A08 A08 A08 A09 A07 DIOA03* A08 A07 DIOA02* A06 A07 A07 DIOA01* A07 A08 A08 A08 A08 A08 A08 A08 A08 A09 A08 A08 A09 A07 DIOA01* A08 A08 A08 A08 A08 A09 A07 DIOA01* A08	DIOC06 I	B15				A15	DIOA06
DIOCOS B13 GND B12 DIOCO4 B11 GND B10 DIOCO3 B09 GND B08 DIOCO2 B07 GND B06 DIOCO1 B05 GND B06 DIOCO1 B05 GND B04 A07 DIOCO2 B07 A08 GND B06 DIOCO1 B05 GND B04 A08 A07 DIOCO2 B07 A08 A08 A08 A07 DIOA02* A08 A08 A08 A09 A09 A07 DIOA01* A07 DIOA01* A07 A08 A08 A08 A08 A08 A09 A09 A09 A09 A09 A09 A09 DIOA01* A07 DIOA01* A07 DIOA01* A08 A09 A09 A09 DIOA01* A07 DIOA01*						A14	
GND B12 DIOCO4 B11 GND B10 DIOCO3 B09 GND B08 DIOCO2 B07 GND B06 DIOCO1 B05 GND B06 DIOCO1 B05 GND B06 A07 GND B06 A07 DIOA02* A06 A07 A07 A08 A08 A07 A08 A08 A07 A08					1		
GND B10 DIOC03 B09 GND B08 DIOC02 B07 GND B06 DIOC01 B05 GND B04 GND A07 DIOA02 * A06 GND A07 DIOA01 * A07 DIOA01	GND I	B12				A12	GND
GND B10 DIOC03 B09 GND B08 DIOC02 B07 GND B06 DIOC01 B05 GND B04 GND A07 DIOA02 * A06 GND A07 DIOA01 * A07 DIOA01						A11	
DIOC03 B09 B01 B01 A01 A09 DIOA03 *						A10	
GND B08 B01 B01 A01 A08 GND A07 DIOA02 * A06 GND B06 DIOC01 B05 GND B04 A04 GND A05 DIOA01 * A04 GND A05 DIOA01 * A05 DIOA01 * A04 GND A05 DIOA01 * A				$\vdash $			
DIOCO2 B07 1961 148 A07 DIOA02 * A06 GND B05 A05 DIOA01 * A05 DIOA01 * A07 DIOA01 * A07 DIOA01 * A08 DIOA01 * A08 DIOA01 * A09 DIOA02 * A09 DIO			B01		A01	A08	
GND B06 A06 GND			_	[96] [48]	1		
DIOC01 B05 A05 DIOA01 * GND B04 A04 GND				_	\mathcal{L}	A06	
GND B04 A04 GND							
						A04	
DIOC00 B03 A03 DIOA00*						A03	DIOA00*
N.C. B02 A02 N.C.							
N.C. B01 A01 N.C.							

- [] shows the pin No. of HONDA TSUSHIN KOGYO CO., LTD. specification. * Can be used as an interrupt signal when used as general-purpose I/O.

DIOA00 - DIOA07	I/O signal DIOA00 - DIOA07 DIOA00 - DIOA03 can be used as interrupt signal DIOIn00 - DIOIn03 at the time of general-purpose I/O.
DIOA00 - DIOA07	I/O signal DIOA00 - DIOA07
DIOB00 - DIOB07	I/O signal DIOB00 - DIOB07
DIOC00 - DIOC07	I/O signal DIOC00 - DIOC07
DIOD00 - DIOD07	I/O signal DIOD00 - DIOD07
EXTCLK0 - EXTCLK1	External clock input
EXTSTARTO - EXTSTART1	External start signal
EXTSTOP0 - EXTSTOP1	External stop signal
EXTREQ0 - EXTREQ1	REQ signal
EXTACK0 - EXTACK1	ACK signal
GND	This is connected to GND of slot.
N.C.	This pin is left unconnected.

Connection method to the external device -Data I/O-

Connecting the data I/O signal(DIOAO* - DIODO*)

These lines input from and output to external devices and can be configured in 16bit with the software.

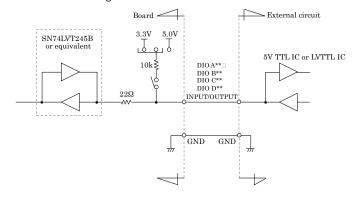
Input and output and setting procedures are the same whether these lines are used for general-purpose digital I/O or bus master transferring and they can be configured in three different settings as shown below:

I/O signal

Signal name	Setup1	Setup2	Setup3
DIOA00 - DIOA07	Input	Input	Output
DIOB00 - DIOB07	Input	Input	Output
DIOC00 - DIOC07	Input	Output	Output
DIOD00 - DIOD07	Input	Output	Output

When settings 1 and 2 are used for general-purpose digital I/O, DIOA00 through DIOA03 can be used as interrupts (rising edge).

Detailed Data I/O Signal Circuit



Connection method to the external device -Control I/O-

Connection to the control signal (EXT**)

In order to control bus mastering from outside, five signals are provided each for pattern I/O. Before using the signals to be input as control signals please verify their pulse widths.

"0" at the end of a signal name indicates a pattern input signal and "1" a pattern output signal.

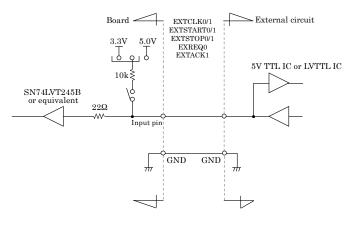
Control signal

Signal name	Direction	Usage	Signal name	Direction	Usage
EXTCLK0	In	Pattern input clock	EXTCLK1	In	Pattern output clock
EXTSTART0	In	Pattern input start signal	EXTSTART1	In	Pattern output start signal
EXTSTOP0	In	Pattern input stop signal	EXTSTOP1	In	Pattern output stop signal
EXTREQ0	In	Pattern input REQ signal	EXTREQ1	Out	Pattern output REQ signal
EXTACK0	Out	Pattern input ACK signal	EXTACK1	In	Pattern output ACK signal

■ DIO-32DM3-PE ■

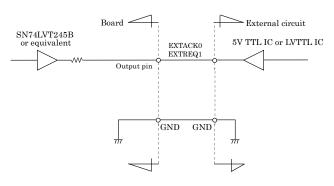
Detailed Control Input Signal Circuit

Control signals to be input include clock, start, stop, and handshake input signals.



Detailed Control Output Signal Circuit

Control signals to be output include handshake output signals.

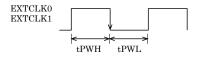


What is the Control Signal?

External clock signal (EXTCLKO/EXTCLK1)

These signals input external pacer clocks. The maximum frequency is $20\mbox{MHz}.$

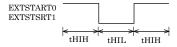
When the external clock input is set as the clock source, pattern input or output occurs at the falling edge of this signal.



tPWH: Clock pulse high width 25ns (Min.) tPWL: Clock pulse low width 25ns (Min.)

Eternal start signal (EXTSTARTO/EXTSTART1)

These input signals start bus mastering with an external signal. The signal level is LVTTL and you can select and enable the rising or falling edge with the software. In order to detect the signal edge, a high- and low-level hold time of 25ns is needed at minimum.



tHIH: High level hold time 25ns (Min.) tHIL: Low level hold time 25ns (Min.)

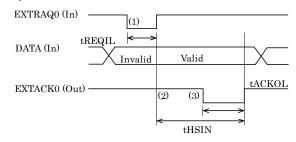
External stop signal (EXTSTOPO/EXTSTOP1)

These input signals stop bus mastering with an external signal. The signal is LVTTL level and you can select and enable the rising or falling edge with the software. In order to detect the signal edge, a high- and low-level hold time of 50ns is needed at minimum.

Handshake Signal (EXTREQO/EXTACKO/ EXTREQ1/EXTACK1)

These signals handshake with external devices. The signal is LVTTL level and controlled with negative logic.

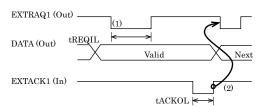
Input



tREQIL: EXTREQO low width 25ns (Min.) tACKOL: EXTACKO low width 100ns tHSIN: Handshaking time 100ns (Min.)

- (1) After setting the handshaking operation, this product samples the EXTREQO signal and starts pattern input when it recognizes a low pulse of more than 50ns. Pattern data prior to that time is disabled.
- (2) The board generates a cycle to write data input from an external device to the PC memory by bus mastering.
- (3) At the end of writing data, the board outputs acknowledge signal EXTRACKO to notify the external device.

Output



tREQOL: EXTREQ1 low width 100ns tACKOL: EXTACK1 low width 25ns (Min.)

- (1) After setting the handshaking operation, this product outputs the EXTREQ1 signal.
- (2) The board begins sampling acknowledge signals from external devices. The board recognizes the end with a low pulse of more than 25ns and, at the leading edge, starts preparing to output the next data.

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Differences between DIO-32DM3-PE, DIO-32DM2-PE, DIO-32DM-PE and PIO-32DM(PCI)

Differences between DIO-32DM3-PE and PIO-32DM(PCI)

	DIO-32DM3-PE	PIO-32DM(PCI)
Input format	Unisolated LVTTL level (Equivalent to 74LVT245B) (positive logic) * 5V TTL level input enabled	Unisolated TTL level (Equivalent to 74ALS245A) (positive logic)
Pull-up	None/3.3V/5V	5V
Output format	Unisolated LVTTL level (Equivalent to 74LVT245B) (positive logic)	Unisolated TTL level (Equivalent to 74ALS245A) (positive logic)
Response time	20nsec	50nsec
Control signal	Unisolated LVTTL level (Equivalent to 74LVT245B) Unisolated LVTTL level (Equivalent to 74LVT245B) * 5V TTL-level input enabled * 3.3V / 5V pull-up can be set	Unisolated TTL level (Equivalent to 74ALS245A) Unisolated TTL level (Equivalent to 74LS125A)
Bus specification	PCI Express Base Specification Rev.2.0 x1	PCI(32bit, 33MHz, Universal key shapes supported)
Operating voltage	3.3V 600mA (Max.) , 12V 30mA (Max.)	5V 700mA (Max.)

Differences between DIO-32DM3-PE, DIO-32DM2-PE and DIO-32DM-PE $\,$

	DIO-32DM3-PE	DIO-32DM2-PE	DIO-32DM-PE				
Input format	Unisolated LVTTL level (Equivalent to 74LVT245B) (positive logic) * 5V TTL level input enabled	Unisolated LVTTL level (Equivalent to 74LV245A) (positive logic) * 5V TTL level input enabled	Unisolated LVTTL level (Equivalent to 74LV245A) (positive logic) * 5V TTL level input enabled				
Pull-up	None/3.3V/5V	None/3.3V/5V	None				
Output format	Unisolated LVTTL level (Equivalent to 74LVT245B) (positive logic)	Unisolated LVTTL level (Equivalent to 74LV245A) (positive logic)	Unisolated LVTTL level (Equivalent to 74LV245A) (positive logic)				
Response time	20nsec	50nsec	50nsec				
Control signal	Unisolated LVTTL level (Equivalent to 74LVT245B) Unisolated LVTL level (Equivalent to 74LV125A) * 5V TTL-level input enabled * 3.3V / 5V pull-up can be set	Unisolated LVTTL level (Equivalent to 74LV245A) Unisolated LVTTL level (Equivalent to 74LV125A) * 5V TTL-level input enabled * 3.3V / 5V pull-up can be set	Unisolated LVTTL level (Equivalent to 74LV245A) Unisolated LVTTL level (Equivalent to 74LV125A) * 5V TTL-level input enabled				
Bus specification	PCI Express Base Specification Rev.2.0 x1	PCI Express Base Specification Rev.1.0a x1	PCI Express Base Specification Rev.1.0a x1				
Operating voltage	3.3V 600mA (Max.) , 12V 30mA (Max.)	3.3V 400mA (Max.) , 12V 30mA (Max.)	3.3V 400mA (Max.)				

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