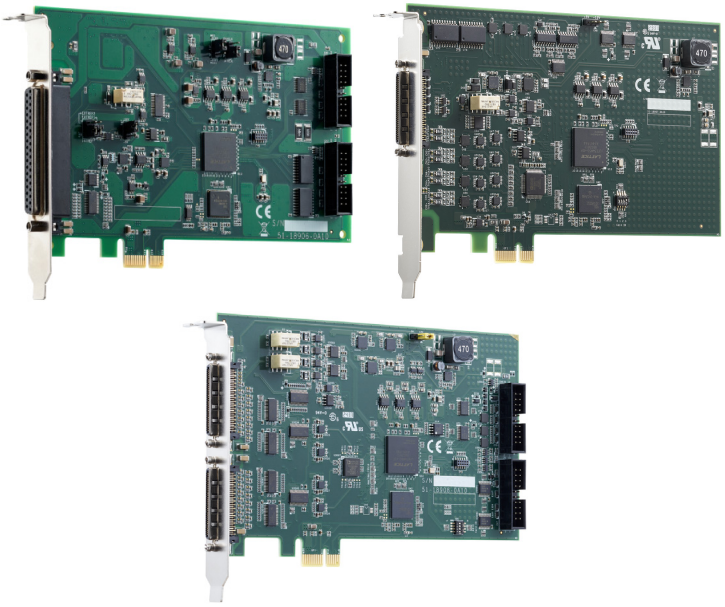
NuDAQ® PCIe-9100 Series

Multiplexer/Simultaneous Multifunction Data Acquisition Card

User's Manual



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LEADING EDGE COMPUTING

Revision History

Revision	Release Date	Description of Change(s)
1.0	2023-02-21	Initial release
1.1	2023-06-01	Update product name to PCIe-9100 Series. Add PCIe-9103.
1.2	2024-05-05	Add PCIe-9146 and PCIe-9147.
1.3	2024-12-24	Add PCIe-9161, PCIe-9163, and PCIe-9164

Preface

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Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

Additional information, aids, and tips that help users perform tasks.

Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

The PCIe-9100 Series of products are PCI Express multifunction data acquisition cards for industrial applications. The plug and play feature of the PCI Express bus architecture makes it easy for users to quickly install PCIe-9100 Series products on their systems.

1.1 Functions

The PCIe-9100 Series provides the following functions for most measurement and control uses:

- 14/16-bit A/D conversion
- 16-bit D/A conversion
- Digital Input/Output lines
- Timer Counter with PWM function
- Encoder

1.2 Features

The PCIe-9100 Series provides the following advanced features:

- A/D conversion
  - Differential (SE) or Differential (SE) input channels
  - 14/16-bit analog input resolution
  - Up to 4M sampling rate
  - Up to onboard 8K samples A/D FIFO memory
  - Programmable Gain Control (x1, x2, x4, x8, x16, x32)
  - Auto-scanning channel selection
  - A/D Data transfer: software polling & bus-mastering DMA with Scatter/Gather functionality
  - 6 trigger mode support, Post trigger, Pre-trigger, Delay trigger, Middle trigger, Post trigger with re-trigger, delay trigger with re-trigger

- D/A conversion
  - Up to 4 channels D/A output with waveform generation capability
  - Up to 2MHz D/A sampling rates
  - 1K samples output data FIFO for DA channels
  - D/A Data transfer: software update and bus-mastering DMA with Scatter/Gather functionality
  - 2 trigger modes: Post trigger, Post trigger with re-trigger
- Digital I/O Lines
  - 16 TTL compatible digital output channels
  - 16 TTL compatible digital input channels
  - 8mA high current driving capability per channel
  - 16 isolated digital output channels (PCIe-9103 only)
  - 16 isolated digital input channels (PCIe-9103 only)
- Timer counter
  - Up to 4 independent programmable 32-bit timer counters
  - Provides one pulse output, PWM output, event counting, and the measurement of frequency and pulse width
- Board ID switch
  - Built-in DIP switch that helps define each card's ID when multiple PCIe-9100 Series cards have been installed on the same PC
- Encoder
  - 2-ch 4 MHz dedicated encoder inputs
  - Supports AB phase and CW/CCW
- PM (Pattern Match) function
  - Reflective actions by comparing patterns of digital input or encoder without involving software

1.3 Applications

- ATE
- Cable Testing
- Laboratory Automation
- Industrial process control and monitoring
- Vibration and transient analysis
- Power monitoring
- Biotech measurement
- Medical instrumentation
- Energy

1.4 Specifications

1.4.1 General Specifications

Model		PCIe-9101/9121/9141	PCIe-9103	PCIe-9161-9163-9164	PCIe-9146/9147
Analog Input					
Simultaneous/Scanning		Scanning			Simultaneous
Number of Channels		16 single-ended (SE) or 8 differential input (DI)	32 single-ended (SE) or 16 differential input (DI)	PCIe-9161: 16-ch PCIe-9163: 32-ch PCIe-9164: 64-ch single-ended (SE) or PCIe-9161: 8-ch PCIe-9163: 16-ch PCIe-9164: 32-ch differential input (DI)	PCIe-9146: 4-ch PCIe-9147: 8-ch differential input (DI)
Max. Sampling Rate	Single-channel	PCIe-9101: 250 kS/s PCIe-9121: 800 kS/s PCIe-9141: 1 MS/s	500 kS/s	4 MS/s	1 MS/s
	Scanning	PCIe-9101: 100 kS/s PCIe-9121: 400 kS/s PCIe-9141: 500 kS/s		1 MS/s *1	
*1: The PCIe-9161 is a 16-ch multiplexer DAQ with a 1MSps sampling rate. It can also function as a 2-ch simultaneous DAQ with a 4MSps sampling rate. The PCIe-9163/9164 is a 32/64-ch multiplexer DAQ with a 1MSps sampling rate. It can also function as a 4-ch simultaneous DAQ with a 4MSps sampling rate.					
Resolution		PCIe-9101/9141: 16-bit PCIe-9121: 14-bit	16-bit		
Input Range		±10V, ±5V, ±2.5V, ±1.25V, ±0.625V, ±0.3125V			
FIFO Buffer Size		Onboard 4K samples		Onboard 8K samples	Onboard 4K samples
Input Coupling		DC			
Input Impedance		10MΩ			1GΩ
Overvoltage Protection		Continuous ±20V	Continuous ±15V		Continuous ±30V
Channel Gain Queue Configuration Size		PCIe-9101/9121: 512 samples PCIe-9141: 1024 samples	512 samples	1024 samples	N/A
Time Base		Internal: 64 MHz External: 8 MHz (CN3 Pin 37)	Internal: 64 MHz External: N/A	Internal: 64 MHz External: 8 MHz (CN1 Pin 32)	Internal: 64 MHz External: 8 MHz (CN1 Pin 16)
Trigger Source		Software Trigger, Analog Trigger, External Digital Trigger (CN3 Pin 17)	Software Trigger, External Trigger (CN4 pin 8)	Software Trigger, Analog Trigger, External Digital Trigger (CN1 Pin 67)	Software Trigger, Analog Trigger, External Digital Trigger (CN1 Pin 53)
Trigger Modes		Pre-trigger, Post trigger, Delay trigger, Middle trigger, Post trigger with re-trigger, Delay trigger with re-trigger			
Data Transfers		Programmed I/O, bus-mastering DMA with scatter/ gather			
Signal-to-Noise Ratio (SNR)		PCIe-9101/9141: 90 dB PCIe-9121: 84 dB	90 dB	84 dB	80 dB
ENOB		PCIe-9101/9141: 14.5 bit PCIe-9121: 13.5 bit	14.5 bits	14 bits	13.5 bits
Offset Error (mV)		PCIe-9101/9141: 0.1 PCIe-9121: 0.3	0.1	0.3	0.1

Table 1-1: General Specifications

Model	PCIe-9101/9121/9141	PCIe-9103	PCIe-9161-9163-9164	PCIe-9146/9147
Gain Error (% of FSR)	0.1			
Integral Nonlinearity (INL)	<1 LSB			
Differential Nonlinearity (DNL)	<1 LSB			
CMRR @ 60 Hz	85 dB			
Analog Output (AO)				
Number of Channels	2	N/A	PCIe-9161: 2 PCIe-9163: 4 PCIe-9164: 4	2
Max. Updating Rate	1MS/s	N/A	2MS/s	1MS/s
Resolution	16-bit	N/A	16-bit	
Output Range	±10 V	N/A	±10 V	
FIFO Size	1K samples (2-ch sharing)	N/A	2K samples (2/4-CH sharing)	1K samples (2-ch sharing)
Output Driving Capacity	±20 mA max	N/A	±20 mA max	
Slew Rate	10 V/µs	N/A	10 V/µs	
Output Coupling	DC	N/A	DC	
Settling Time (0.1% of full scale)	2 µs	N/A	2 µs	
Output Impedance	<0.1 ohms	N/A	<0.1 ohms	
SNR	>100 dB	N/A	>100 dB	
THD	>75 dB	N/A	>75 dB	
Offset Error	±0.1 mV	N/A	±0.1 mV	
Gain Error	±0.05% of FSR	N/A	±0.05% of FSR	
INL (Relative Accuracy)	±2 LSB max	N/A	±2 LSB max	
DNL	±1 LSB	N/A	±1 LSB	
Default On/Off	AO Off (relay) if AO relay turned on, default AO is 0V (+0.1V to -0.1V)	N/A	AO Off (relay) if AO relay turned on, default AO is 0V (+0.1V to -0.1V)	
Power On/Off Glitch	<1mV/µs	N/A	<1mV/µs	
Timebase Source	Internal Timebase fixed 64MHz External Timebase fixed 8MHz (CN3.37)	N/A	Internal Timebase fixed 64MHz External Timebase fixed 8MHz (CN1.32)	Internal Timebase fixed 64MHz External Timebase fixed 8MHz (CN1.16)
Trigger Source	Software trigger External digital trigger (CN3.17)	N/A	Software trigger External digital trigger (CN1 Pin 33)	Software trigger External digital trigger (CN1 Pin 54)
Trigger Modes	Post trigger Post trigger with re-trigger	N/A	Post trigger Post trigger with re-trigger	
Data Transfers	Programmed I/O bus-mastering DMA with scatter/ gather	N/A	Programmed I/O bus-mastering DMA with scatter/ gather	
General Purpose Digital IO (DIO)				
Number of Channels	Digital Input: 16 channels Digital Output: 16 channels			

Table 1-1: General Specifications

Model	PCIe-9101/9121/9141	PCIe-9103	PCIe-9161-9163-9164	PCIe-9146/9147
Digital Type	TTL	Isolation 2500Vrms	TTL	
Power-on Status	Digital Input: Low Digital Output: Low	Digital Input: Low Digital Output: Open	Digital Input: Low Digital Output: Low	
FIFO Buffer Size	512 samples for all DI channels 512 samples for all DO channels	N/A	1024 samples for all DI channels 1024 samples for all DO channels	512 samples for all DI channels 512 samples for all DO channels
DI Input Logic Level	Logic Low: VIL =0V - 0.8V (max.); IIL = -0.2 mA max. Logic High: VIH = 2.0V (min.) - 5V; IIH = 20 mA max.	Logic low: VIL =0V - 1.5V(max); IIL =- 0.2 mA max. Logic high: VIH = 5V(min) - 24V; IIH = 10 mA max.	Logic Low: VIL =0V - 0.8V (max.); IIL = -0.2 mA max. Logic High: VIH = 2.0V (min.) - 5V; IIH = 20 mA max.	
DI Input Frequency Range	Up to 500ns pulse for 1MHz Duty 50% sync by DI_SYNC_IN (CN1 Pin 20) up to 1MHz Down to 0.01Hz	N/A	Up to 500ns pulse for 1MHz Duty 50% sync by DI_SYNC_IN (CN8 Pin 20) up to 1MHz Down to 0.01Hz	Up to 500ns pulse for 1MHz Duty 50% sync by DI_SYNC_IN (CN1 Pin 59) up to 1MHz Down to 0.01Hz
DI Input Impedance	pull-low 100kohm	2.4kohm/0.5W	pull-low 100kohm	
DI DMA Sync IN source	1. Up to 1MHz from Internal Timebase 2. Up to 1MHz from External Timebase fixed 8MHz (CN3.37) 3. Up to 1MHz from DI SYNC IN (CN1 Pin 20)	N/A	1. Up to 1MHz from Internal Timebase 2. Up to 1MHz from External Timebase fixed 8MHz (CN1 Pin 32) 3. Up to 1MHz from DI (CN8 Pin 20)	1. Up to 1MHz from Internal Timebase 2. Up to 1MHz from External Timebase fixed 8MHz (CN1 Pin 16) 3. Up to 1MHz from DI SYNC IN (CN1 Pin 59)
DO Output Logic Level	Logic low: VIL = 0V - 0.5V (max.); OIL = 8mA max. Logic high: VIH = 2.4V (min.); OIH = 0.4mA max.	Logic low: VIL = Open; Sink current = 800mA max per CH & total = 1.6A max for 16-ch Logic high: VIH = 5V (min) - 35V from Iso VDD	Logic low: VIL = 0V - 0.5V (max.); OIL = 8mA max. Logic high: VIH = 2.4V (min.); OIH = 0.4mA max.	
DO Output Speed	Up to 500ns pulse for 1MHz Duty 50% sync by DO_SYNC_OUT (CN2 Pin 20) up to 1MHz Down to 0.01Hz	N/A	Up to 500ns pulse for 1MHz Duty 50% sync by DO_SYNC_OUT (CN7 Pin 20) up to 1MHz Down to 0.01Hz	Up to 500ns pulse for 1MHz Duty 50% sync by DO_SYNC_OUT (CN1 Pin 68) up to 1MHz Down to 0.01Hz
DO Pull-low	Pull-low 100kohm	No, default Open	Pull-low 100kohm	
DO Default Level	Low			
DO DMA Sync OUT source	1. Up to 1MHz from Internal Timebase 2. Up to 1MHz from External Timebase fixed 8MHz (CN3.37)	N/A	1. Up to 1MHz from Internal Timebase 2. Up to 1MHz from External Timebase fixed 8MHz (CN1 Pin 32)	1. Up to 1MHz from Internal Timebase 2. Up to 1MHz from External Timebase fixed 8MHz (CN1 Pin 16)
DIO Setup Time	250 ns	N/A	250 ns	
DIO Hold Time	250 ns	N/A	250 ns	

Table 1-1: General Specifications

Model	PCIe-9101/9121/9141	PCIe-9103	PCIe-9161-9163-9164	PCIe-9146/9147
Trigger Source	Software trigger, External digital trigger (CN3.17)	Software trigger, External digital trigger (CN4.8)	Software trigger, External digital trigger (CN7 Pin 19 for DI, CN7 Pin 17 for DO)	Software trigger, External digital trigger (CN1 Pin 53 for DI, CN1 Pin 54 for DO)
Trigger Modes	Post trigger Post trigger with re-trigger			
Data Transfers	Programmed I/O, Bus-mastering DMA with scatter/ gather	Programmed I/O	Programmed I/O, Bus-mastering DMA with scatter/ gather	
General Purpose Timer/Counter (GPTC)				
Number of Channels	2 on CN3	1 on CN4		2 on CN1
Resolution	32-bit			
Clock Source	1. Internal Timebase [fixed 33MHz] 2. External Timebase 0.01Hz-8MHz (CN3.37)	1. Internal Timebase[fixed 33MHz] 2. External Timebase fixed 2MHz (CN4.1)	1. Internal Timebase [fixed 33MHz] 2. External Timebase 0.01Hz-8MHz (CN8 Pin 5,6,7,8)	1. Internal Timebase [fixed 33MHz] 2. External Timebase 0.01Hz-8MHz (CN1 Pin 16)
Clock & Gate Input Level	Logic low: VIL = 0V to 0.8V (max). Logic high: VIH = 2.0V (min.)			
Counter Output Level	Logic low: VIL = 0.8V (max.) @ 2.5mA Logic high: VIH = 2.0V (min.) @ -2.5mA			
Overvoltage Protection	0V to 5.5V			
Counter Mode	Mode 1: Simple Gated-Event Counting Mode 2: Single Period Measurement Mode 3: Single Pulse-Width Measurement Mode 4: Single-Gated Pulse Generation Mode 5: Single Triggered Pulse Generation Mode 6: Re-Triggered Single Pulse Generation Mode 7: Single-Triggered Continuous Pulse Generation Mode 8: Continuous Gated Pulse Generation			
PWM	Supported and can change on the fly			
Encoder				
Encoder Input Channels	N/A	N/A	2	
Pinouts	N/A	N/A	CN8.1-12 in Mode 2 (See “Programmable Function I/O” on page 108.)	CN1.17-24 & CN1.51-58 In Mode 2 (See “Programmable Function I/O” on page 108.)
Max. Input Frequency	N/A	N/A	4MHz	
Encoder Count	N/A	N/A	$(2^{31}-1)$ bits	
Encoder Mode	N/A	N/A	1. CW/CCW Encoder Mode 2. X1 Encoder Mode 3. X2 Encoder Mode 4. X4 Encoder Mode	
Data Transfer	N/A	N/A	Polling & DMA DMA: combined AI & non-combined AI	
Mechanical & Environmental				
Bus Type	PCI Express 1.0			
Bus Width	x1 Lane			
Connector	37-pin D-type connector		68-pin SCSI-type female	

Table 1-1: General Specifications

Model	PCIe-9101/9121/9141	PCIe-9103	PCIe-9161-9163-9164	PCIe-9146/9147
Dimensions (mm)	169.55 (L) X 16.15 (W) X 98.4 (H)		181.05 (L) x 21.1 (W) x 126.29 (H)	181.05 (L) x 19.4 (W) x 126.72 (H)
Weight	118.8 g		115 g	100 g
Operating Temperature	0°C to 60°C			
Storage Temperature	-40 to 85 °C			
Humidity	10% to 90%,non-condensing			
ESD	Contact ± 4 kV, Air ± 8 kV			
EMI/EMC	CE & FCC Class B (EN61000-6-4/EN61000-6-2)			

Table 1-1: General Specifications

1.4.2 Performance Specifications

1.4.2.1 Large Signal Bandwidth

Large Signal Bandwidth (-3db with 0.9 of FSR of Input)						
Input Range	**±10V**	**±5V**	**±2.5V**	**±1.25V**	**±0.625V**	**±0.3125V**
PCIe-9101	330kHz	400kHz	470kHz	470kHz	460kHz	470kHz
PCIe-9103	420kHz	720kHz	730kHz	720kHz	730kHz	730kHz
PCIe-9121	380kHz	560kHz	760kHz	750kHz	760kHz	760kHz
PCIe-9141	410kHz	570kHz	700kHz	760kHz	770kHz	770kHz
PCIe-9161	1.26Mhz	1.69MHz	2.11MHz	2.23MHz	2.66MHz	2.93MHz
PCIe-9163						
PCIe-9164						
PCIe-9146	220kHz or 25kHz software selectable					
PCIe-9147						

Table 1-2: Large Signal Bandwidth

1.4.2.2 Small Signal Bandwidth

Small Signal Bandwidth (-3db with 0.1 of FSR of Input)						
Input Range	**±10V**	**±5V**	**±2.5V**	**±1.25V**	**±0.625V**	**±0.3125V**
PCIe-9101	480kHz	480kHz	500kHz	500kHz	515kHz	560kHz
PCIe-9103	1.9MHz	2.75MHz	3.5MHz	3.5MHz	2.3MHz	1.55MHz
PCIe-9121	1.9MHz	2.65MHz	3.5MHz	3.45MHz	2.3MHz	1.69MHz
PCIe-9141	1.9MHz	2.65MHz	3.5MHz	3.45MHz	2.3MHz	1.69MHz
PCIe-9161	2.4MHz	3MHz	2.5MHz	4.5MHz	4.7MHz	4.95MHz
PCIe-9163						
PCIe-9164						
PCIe-9146	220kHz or 25kHz software selectable					
PCIe-9147						

Table 1-3: Small Signal Bandwidth

1.4.2.3 System Noise

System noise (LSBrms)						
Input Range	**±10V**	**±5V**	**±2.5V**	**±1.25V**	**±0.625V**	**±0.3125V**
PCIe-9101	1	1	1	1.5	2	3
PCIe-9103	1	1.5	1.5	2.5	3.5	5
PCIe-9121	1	1	1	1	1	1.5
PCIe-9141	1	1.5	1.5	2.5	3.5	5
PCIe-9161	1.3	1.3	1.3	1.6	2.6	4
PCIe-9163						
PCIe-9164						
PCIe-9146	1.2					1.7
PCIe-9147						

Table 1-4: System Noise

1.4.2.4 CrossTalk

CrossTalk (dB)						
Input Range	**±10V**	**±5V**	**±2.5V**	**±1.25V**	**±0.625V**	**±0.3125V**
PCIe-9101	-80					
PCIe-9103						
PCIe-9121						
PCIe-9141						
PCIe-9161	-90					
PCIe-9163						
PCIe-9164						
PCIe-9146	-100					
PCIe-9147						

Table 1-5: CrossTalk

1.4.2.5 Drift – Offset

Drift – Offset (LSB per C)						
Input Range	**±10V**	**±5V**	**±2.5V**	**±1.25V**	**±0.625V**	**±0.3125V**
PCIe-9101	3	1	2	3	3	3
PCIe-9103	2	1	1	1	1	1
PCIe-9121	2	1	1	1	1	1
PCIe-9141	3	3	1	2	1	2
PCIe-9161	0.5					
PCIe-9163						
PCIe-9164						
PCIe-9146	1					
PCIe-9147						

Table 1-6: Drift – Offset

1.4.2.6 Drift – Gain

Drift – Gain (LSB per C)						
Input Range	**±10V**	**±5V**	**±2.5V**	**±1.25V**	**±0.625V**	**±0.3125V**
PCIe-9101	1	1	1	1	1	1
PCIe-9103	4	4	4	4	4	4
PCIe-9121	4	4	4	4	4	4
PCIe-9141	7	7	7	7	7	6
PCIe-9161	1					
PCIe-9163						
PCIe-9164						
PCIe-9146						
PCIe-9147						

Table 1-7: Drift – Gain

1.4.2.7 Settling Time to Full-scale Step for ±2 LSB

Settling time to full-scale step for ±2 LSB (µs)						
Input Range	**±10V**	**±5V**	**±2.5V**	**±1.25V**	**±0.625V**	**±0.3125V**
PCIe-9101	10					
PCIe-9103	2					
PCIe-9121	2					
PCIe-9141	2					
PCIe-9161	1		1.11	1.25		>2
PCIe-9163						
PCIe-9164						

Table 1-8: Settling Time to Full-scale Step for ±2 LSB

1.4.2.8 Settling Time Error at Maximum Sampling Rate, LSB

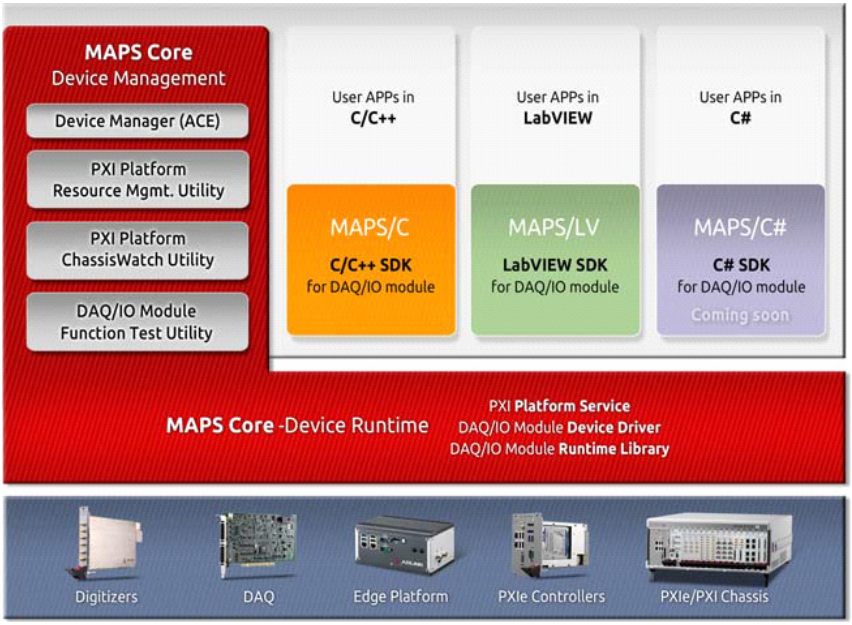
Settling time error at maximum sampling rate, LSB (µs)							
Model	**Input Range**	**±10V**	**±5V**	**±2.5V**	**±1.25V**	**±0.625V**	**±0.3125V**
	Sampling Rate						
PCIe-9101	100k	±2					
PCIe-9103	500k	±2					
PCIe-9121		±2					
PCIe-9141		±2					
PCIe-9161	1M	<=±1	<=±2		<=±3		
PCIe-9163							
PCIe-9164							

Table 1-9: Settling Time Error at Maximum Sampling Rate, LSB

1.5 Software Support

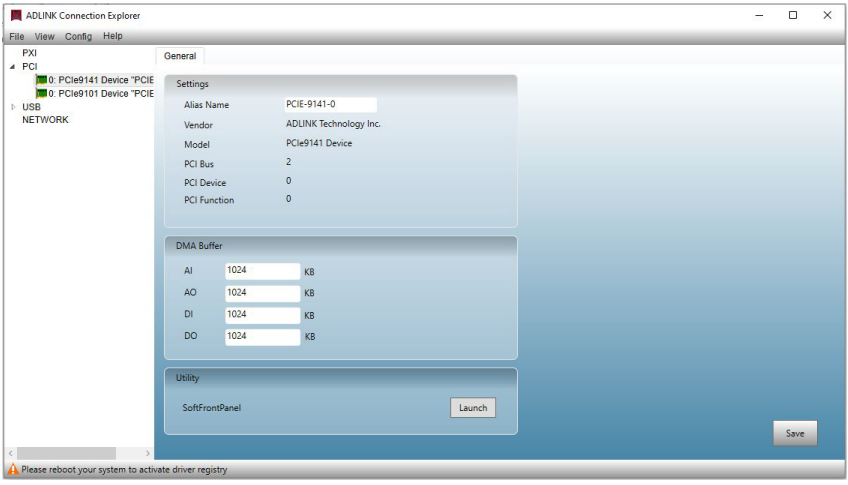
ADLINK provides versatile software drivers and packages to suit various user approaches to building a system. Aside from programming libraries, such as DLLs, for most Windows-based systems, ADLINK also provides drivers for other application environments such as LabVIEW. All software can be downloaded from the ADLINK official website. Commercial software drivers are protected with licensing authorization codes. Without an authorization code, you can install and run the demo version for trial/demonstration purposes for up to two hours. Contact your ADLINK dealer to purchase a software license. ADLINK Measurement, Automation & Platform Service (MAPS) is a software service package designed for data acquisition, automation and PXI platforms.

By leveraging low-level kernel management and a user friendly API, users can easily manage devices under a Windows environment and focus on developing applications.



1.5.1 MAPS Core

ADLINK MAPS Core is a software package that includes all the device drivers for Windows and a system level management tool called ACE (ADLINK Connection Explorer). With MAPS Core installed, the operating system can identify ADLINK devices and assign the necessary resources for low-level access, such as IO read/write or direct memory access. MAPS Core is necessary for all ADLINK DAQ modules. To ensure the user has the latest software, go to the ADLINK product webpage or contact ADLINK technical service. MAPS Core also comes with a system management portal called ADLINK Connection Explorer (ACE). Through ACE, users can discover and manage ADLINK DAQ modules to reserve a certain size of memory buffer for DMA operation or set the user alias name for operating the module in a LabVIEW environment.



ADLINK Connection Explorer (ACE) also provides a ready-to-use soft-front panel for digitizer products. Clicking the Launch button in the "Utility" block allows users to control DAQ cards through the UI and display the acquired waveform/data on the screen.

1.5.2 MAPS/LV, LabVIEW Support

Customers who develop their own programs in LabVIEW must install the MAPS/LV software package. MAPS/LV, also called DAQ-LabVIEW Plus, includes the software library and sample program for LabVIEW. For more information, download and install the latest MAPS/LV software from the following website and refer to the MAPS/LV manual:

https://www.adlinktech.com/Products/Data_Acquisition/DAQSoftware_Utility/MAPS_LV

1.5.3 MAPS/C, C & C++ Support

Customers who develop their own programs in C or C++ environments must install the MAPS/C software package. MAPS/C includes all the software components required for developing applications in C/C++, such as header files, a device API library and versatile sample programs for understanding how to manipulate the device correctly. Find the latest MAPS/C on the ADLINK website.

https://www.adlinktech.com/Products/Data_Acquisition/DAQSoftware_Utility/MAPS_C

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2 Getting Started

This chapter describes the proper installation environment, installation procedures, package contents and basic information users should be aware of.

Diagrams and images of equipment illustrated are for reference only. Actual system configuration and specifications may vary.

2.1 Package Contents

Before continuing, check the package contents for any damage and check if the following items are included in the packaging:

- PCIe-9100 Series Multi-Function Data Acquisition Card
- Product Warranty Card

The card contains electro-static sensitive components that can easily be damaged by static electricity. Therefore, the card should be handled on a grounded anti-static mat. The operator should be wearing an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the card module carton for obvious damage. Shipping and handling may cause damage to your module. Be sure there are no shipping and handling damages on the modules carton before continuing.

After opening the card module carton, extract the system module and place it only on a grounded anti-static surface with component side up.

Inspect the module for any damage. Press down on all the socketed IC's to make sure that they are properly seated. Do this only with the module place on a firm flat surface.

WARNING: DO NOT install or apply power to equipment that is damaged or if there are missing components. Retain the shipping carton and packing materials for inspection. Please contact your ADLINK dealer/vendor immediately for assistance and obtain authorization before returning any product.

2.2 Device Layout and I/O Connectors

2.2.1 PCIe-9101 PCB Layout

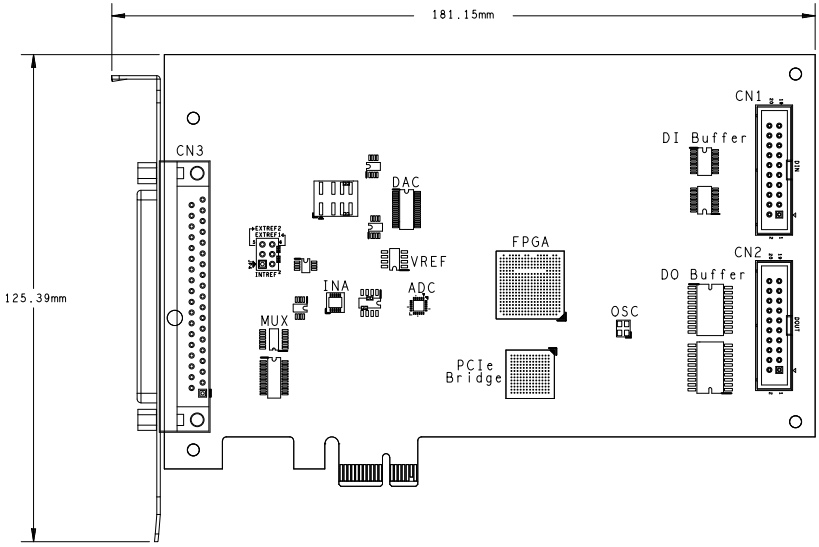


Figure 2-1: PCIe-9101 PCB Front Layout

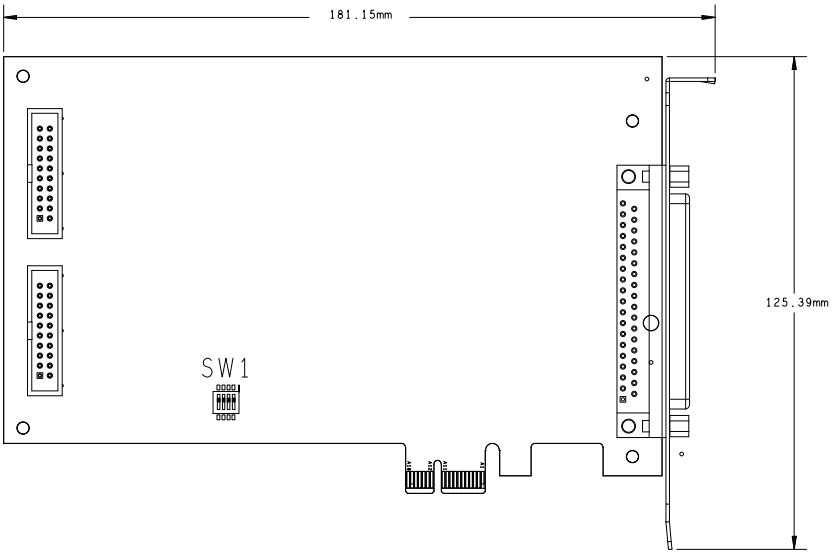


Figure 2-2: PCIe-9101 PCB Rear Layout

2.2.2 PCIe-9103 PCB Layout

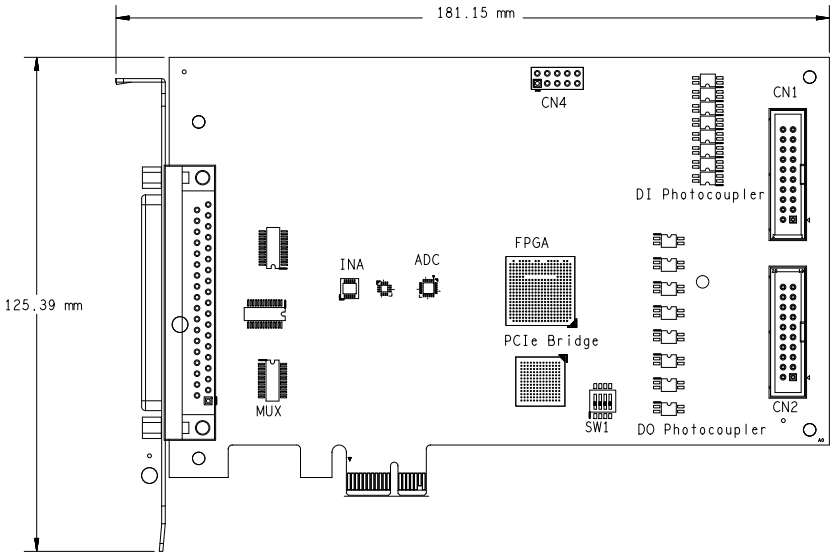


Figure 2-3: PCIe-9103 PCB Layout

2.2.3 PCIe-9121/9141 PCB Layout

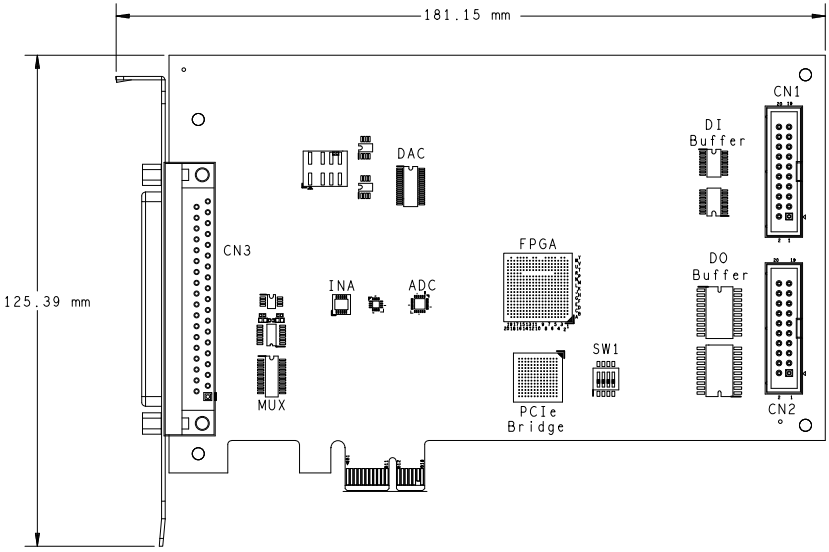


Figure 2-4: PCIe-9121/9141 PCB Layout

2.2.4 PCIe-9146/9147 PCB Layout

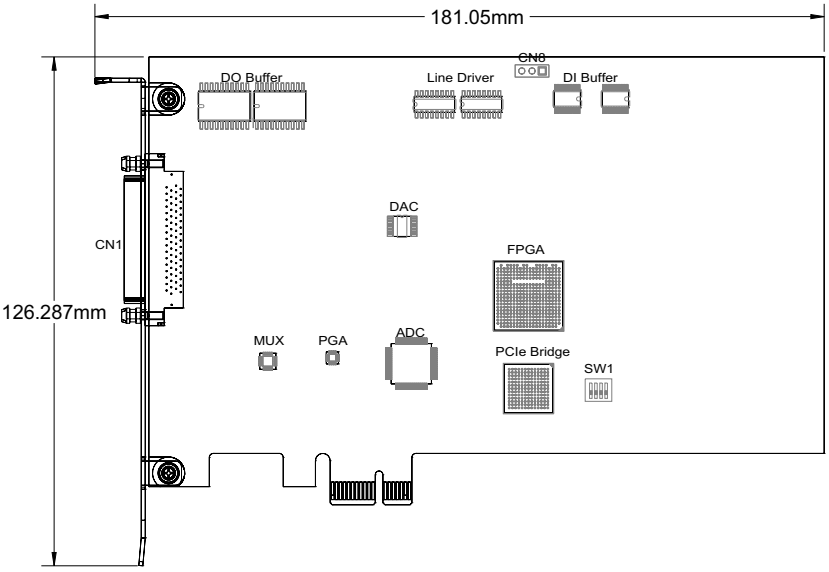


Figure 2-5: PCIe-9146/9147 PCB Layout

2.2.5 PCIe-9161 PCB Layout

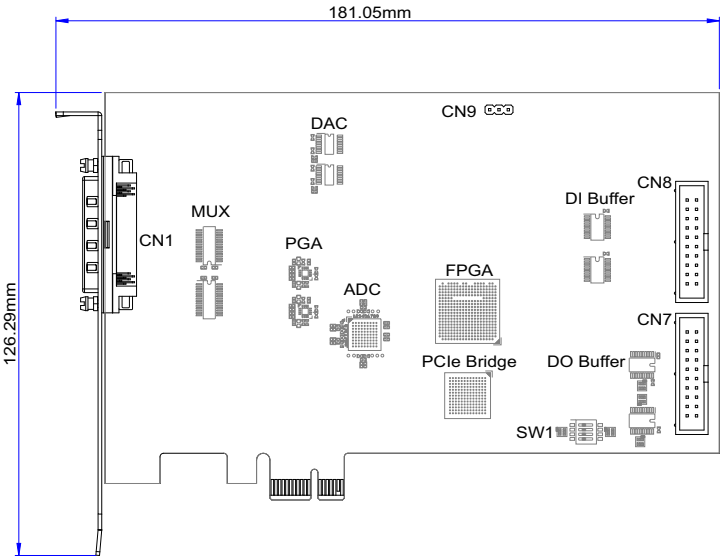


Figure 2-6: PCIe-9161 PCB Front Layout

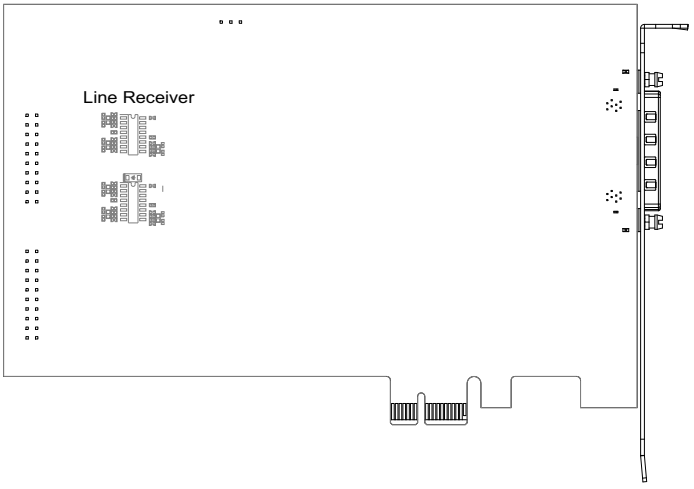


Figure 2-7: PCIe-9161 PCB Rear Layout

2.2.6 PCIe-9163/9164 PCB Layout

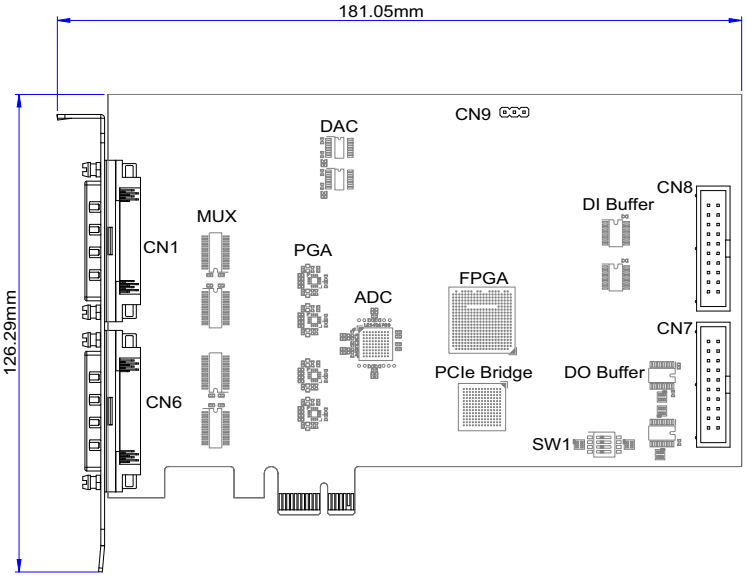


Figure 2-8: PCIe-9163/9164 PCB Front Layout

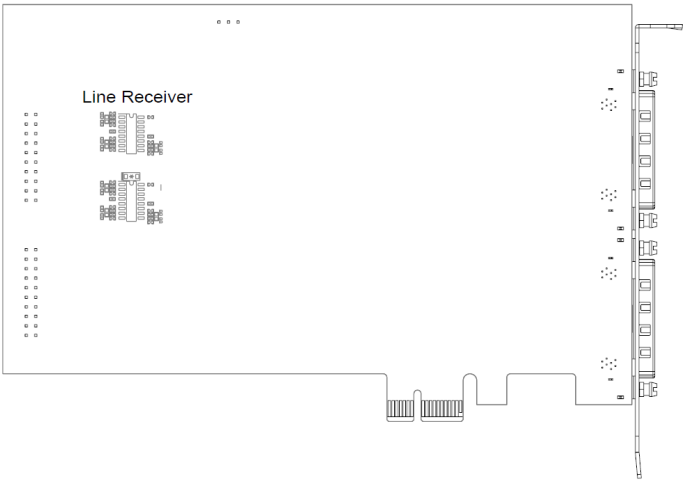


Figure 2-9: PCIe-9163/9164 PCB Rear Layout

2.3 Switch and Jumper Settings

The following item can be configured with jumpers:

- analog output range on PCIe-9101
- 5V or 12V output setting on CN1 Pins 15, 49 on PCIe-9146/9147
- 5V or 12V output setting on CN1 Pins 34 on PCIe-9161/9163/9164

The card's jumpers and switches are preset at the factory. You can change the jumper settings for your own applications.

Configuration	Attributes	Jumper
D/A Reference Source	Internal Reference or External Reference	JP4
5V or 12V output	Output 5V or 12V on CN1 Pins 15, 49	CN8
5V or 12V output	Output 5V or 12V on CN1 Pins 15, 49	CN9

Table 2-1: Jumper Settings

2.3.1 D/A Reference Voltage Settings

The D/A converter's reference voltage source can be supplied both *internally and externally*. The external reference voltage comes from connector CN3, Pin 31 (*ExtRef1*) and Pin12 (*ExtRef2*). The reference source of the D/A channel 1 and channel 2 are selected by JP4.

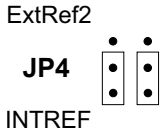
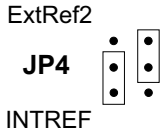
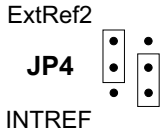
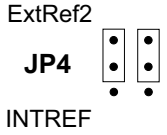
D/A CH1 is Internal D/A CH2 is Internal (Default setting)	
D/A CH1 is External D/A CH2 is Internal	
D/A CH1 is Internal D/A CH2 is External	
D/A CH1 is External D/A CH2 is External	

Table 2-2: D/A Reference Voltage Settings

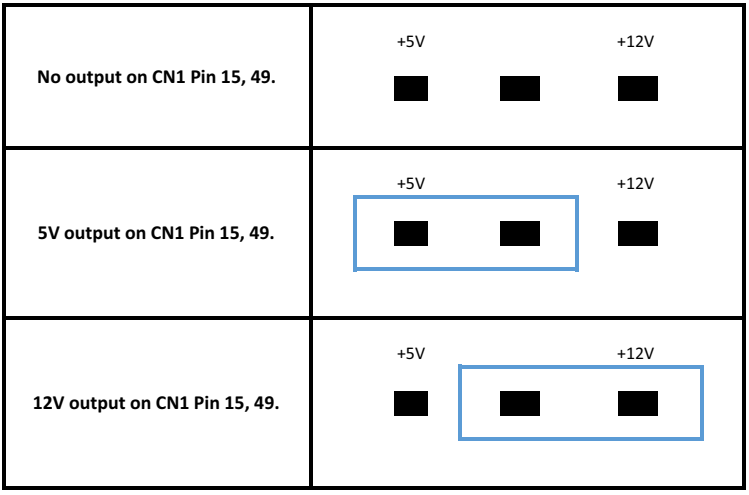


Figure 2-10: PCIe-9146/9147 CN8 Settings

Definition	Pin No,		Definition
	1	35	
	...	...	
	14	48	
+12V or 5V	15	49	+12V or 5V
	...	...	
	34	68	

Table 2-3: PCIe-9146/9147 5V/12V Output Pin on CN1 Pin Assignments

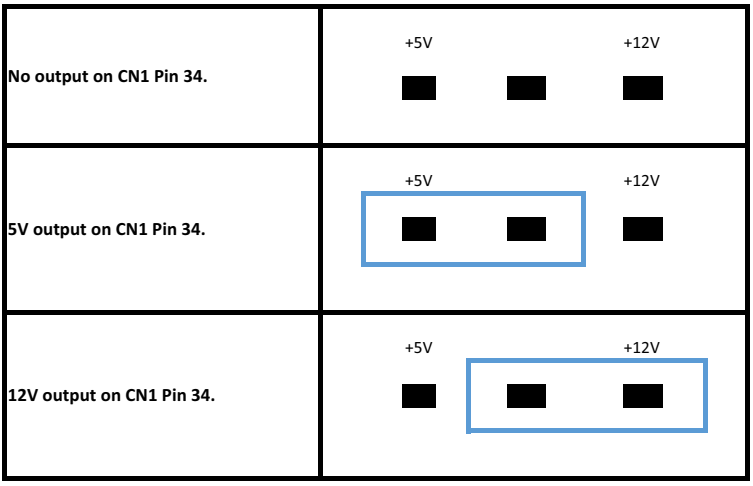


Figure 2-11: PCIe-9161/9163/9164 CN9 Settings

Definition	Pin No,		Definition
	1	35	
	...	...	
	14	48	
	15	49	
	...	...	
+12V or 5V	34	68	DGND

Table 2-4: PCIe-9161/9163/9164 5V/12V Output Pin on CN1 Pin Assignments

2.3.2 Board ID (SW1)

The PCIe-9100 Series has a built-in DIP switch (SW1), which is used to define each card's board ID. When there are multiple cards on the same platform, this board ID switch is useful for identifying each card's device number. After setting each PCIe-9100 Series card, you can identify each card in the system with different device numbers. The default value of the Board ID is 0 and if you need to adjust it to another value, set the SW1 switch as shown in the table below.

Figure 2-12: Board ID SW1 DIP Switch

SW1	Pin 1	Pin 2	Pin 3	Pin 4
Board ID	**ID0**	**ID1**	**ID2**	**ID3**
0	Off	Off	Off	Off
1	On	Off	Off	Off
2	Off	On	Off	Off
3	On	On	Off	Off
4	Off	Off	On	Off
5	On	Off	On	Off
6	Off	On	On	Off
7	On	On	On	Off
8	Off	Off	Off	On
9	On	Off	Off	On
10	Off	On	Off	On
11	On	On	Off	On
12	Off	Off	On	On
13	On	Off	On	On
14	Off	On	On	On
15	On	On	On	On

Table 2-5: Board ID by SW1 Switch

2.4 Connector Pin Assignments

2.4.1 PCIe-9101/9121/9141/9103

The PCIe-9101/9121/9141/9103 comes equipped with two 20-pin insulation displacement connectors (CN1 and CN2) and one 37-pin D-type connector (CN3). CN1 and CN2 are located on the board and CN3 is located on the faceplate.

CN1 is for digital signal input, CN2 is for digital signal output, and CN3 is for analog input/output and timer/counter signals.

2.4.1.1 CN3: Analog Input/Output & Counter/Timer

CN3 is a 37-pin D-type connector with the following pin assignments.

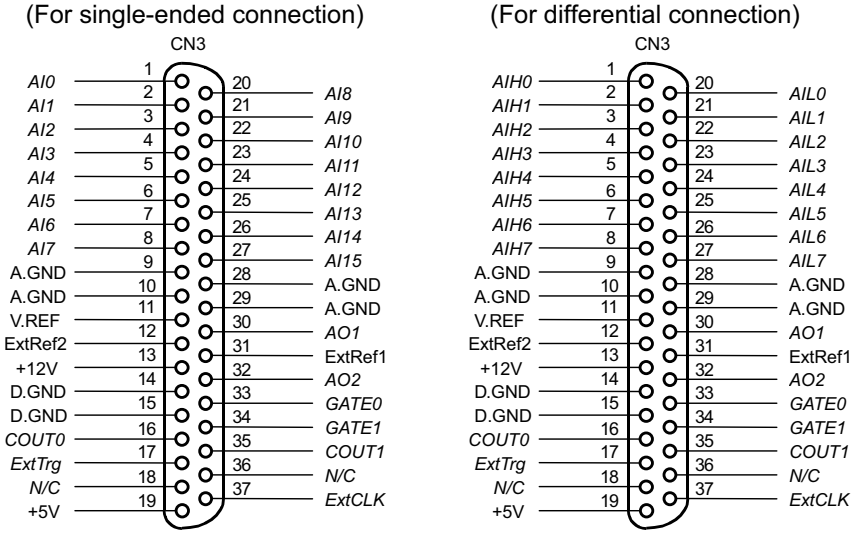


Figure 2-13: PCIe-9101 CN3 Pin Assignments

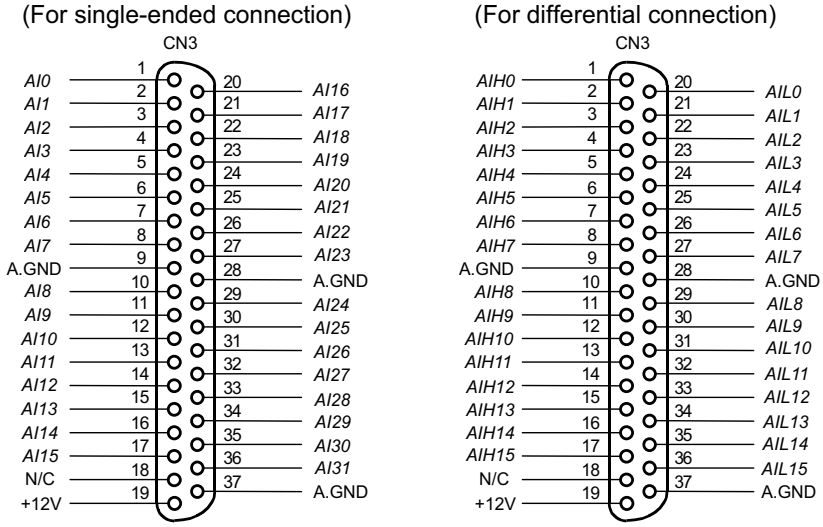


Figure 2-14: PCIe-9103 CN3 Pin Assignments

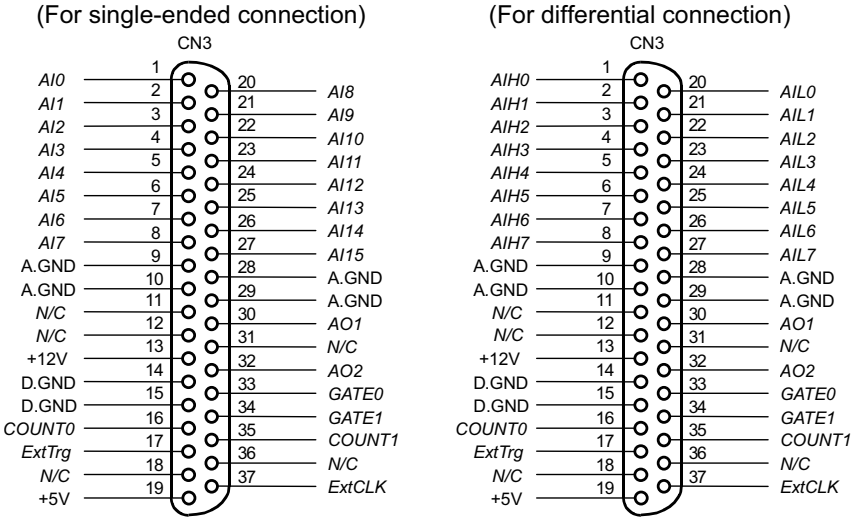


Figure 2-15: PCIe-9121/9141 CN3 Pin Assignments

Signal Name	I/O	Description
AI <0…31>	I	Signal-ended Analog Input Channels 0-31
AIH <0…15>	I	Differential Analog High Input Channels 0-15
AIL <0…15>	I	Differential Analog Low Input Channels 0-15
ExtRef <1,2>	I	External Reference Voltage for D/A CH <1,2>
AO <0,1>	O	Analog Output Channels <0,1>
ExtCLK	I	External Clock
ExtTrig	I	External Trigger Signal
GATE <0,1>	I	Gate Input <0,1>
COUT<0,1>	O	Signal Output of Counter Channels <0,1>
V.REF	O	Voltage Reference
A.GND		Analog Ground
D.GND		Digital Ground
+12V	O	12V power output @ 0.2A
+5V	O	5V power output @ 0.2A
NC		No connect

Table 2-6: CN3 Pin Assignment Legend

2.4.1.2 CN1/CN2: Digital Signal Input/Output

CN1 and CN2 are 20-pin insulation displacement connectors for digital signal input/output with the following pin assignments.

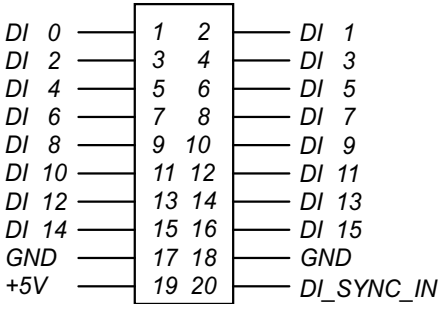


Figure 2-16: PCIe-9101/21/41 CN1 Pin Assignments

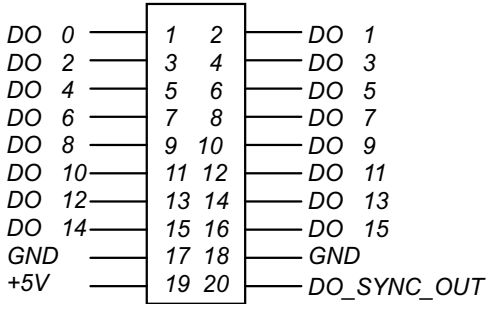


Figure 2-17: PCIe-9101/21/41 CN2 Pin Assignments

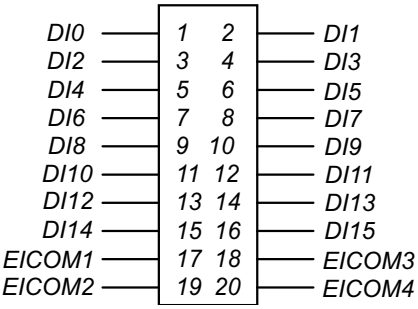


Figure 2-18: PCIe-9103 CN1 Pin Assignments

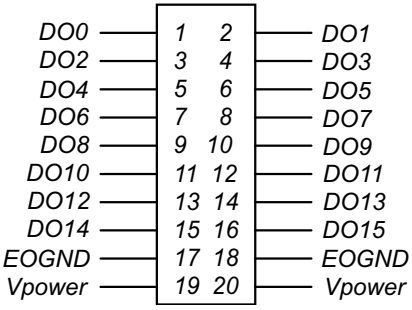


Figure 2-19: PCIe-9103 CN2 Pin Assignments

Signal Name	I/O	Description
DI <0…15>	I	Digital Input signal channels 0-15
DO <0…15>	O	Digital Output signal channels 0-15
DI_SYNC_IN	I	Digital Input synchronization clock source in
DO_SYNC_OUT	O	Digital Output synchronization clock source out
GND		Digital Ground
+12V	O	12V power output @ 0.2A
+5V	O	5V power output @ 0.2A
EICOM<1...4>	I	Common plane for Isolated Input group.
EOGND		Isolated Output Signal Ground.
Vpower	I	Isolated Output driver's power supply. Supports 5 to 35V.

Table 2-7: CN1/CN2 Pin Assignment Legend

2.4.1.3 CN4: External Signal Connector (PCIe-9103 only)

CN4 is a 10-pin connector used for external signal connections with the following pin assignments.

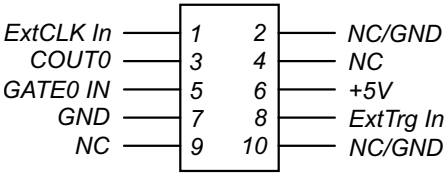


Figure 2-20: CN4 Pin Assignments

Signal Name	I/O	Description
ExtCLK In/CONVS.	I	External Clock or Conversion clock signal input
NC		No Connection
GATE	I	External Gate Control Signal

Table 2-8: CN4 Pin Assignment Legend

Signal Name	I/O	Description
COUT	O	Output of Counter
ExtTrg In	I	External A/D Trigger Signal
+5V	O	+5V output
GND		Ground

Table 2-8: CN4 Pin Assignment Legend

2.4.2 PCIe-9146/9147

The PCIe-9146/9147 comes equipped with one 68-pin SCSI-type female connector (CN1). CN1 is located on the faceplate which is used for analog input/output, digital signal input/output, timer/counter signals and encoder signals.

2.4.2.1 PCIe-9146/9147 CN1 Connector

CN1 is a 68-pin SCSI-type connector with the following pin assignments.

NC	1	35	NC
AI_AO_CaI+	2	36	AI_AO_Cal-
NC	3	37	NC
NC	4	38	NC
AGND	5	39	AGND
NC	6	40	NC
AIH3	7	41	AIL3
AGND	8	42	AGND
AIH2	9	43	AIL2
AIH1	10	44	AIL1
AGND	11	45	AGND
AIH0	12	46	AIL0
AO1	13	47	AGND
AO0	14	48	AGND
+12V or 5V	15	49	+12V or 5V
Ext. Time Base or GPTC CLK0	16	50	Ext. CONVSN. or GPTC CLK1
DI0 / DI0 / EA0+	17	51	DI8 / GPTC GATE0 / EA0-
DI1 / DI1 / EB0+	18	52	DI9 / GPTC GATE1 / EB0-
DI2 / DI2 / EZ0+	19	53	DI10 / AI Trigger In/ EZ0-
DI3 /DI3 / EORG0+	20	54	DI11 / AO Trigger In / NA
DI4 / DI4 / NA	21	55	DI12 / NA / EORG1
DI5 / DI5 / EA1+	22	56	DI13 / NA / EA1-
DI6 / DI6 / EB1+	23	57	DI14 / NA / EB1-
DI7 / DI7 / EZ1+	24	58	DI15 / NA / EZ1-
DGND	25	59	DI Sync In
DO0	26	60	DO8 / GPTC COUT0 / DO8
DO1	27	61	DO9 / GPTC COUT1 / DO9
DO2	28	62	DO10 / NA / DO10
DO3	29	63	DO11 / NA / DO11
DO4	30	64	DO12 / NA / DO12
DO5	31	65	DO13 / NA / DO13
DO6	32	66	DO14 / NA / DO14
DO7	33	67	DO15 / NA / DO15
DGND	34	68	DO Sync Out

Figure 2-21: PCIe-9146 CN1 Pin Assignments

AIH7	1	35	AIL7
AI_AO_Cal+	2	36	AI_AO_Cal-
AIH6	3	37	AIL6
AIH5	4	38	AIL5
AGND	5	39	AGND
AIH4	6	40	AIL4
AIH3	7	41	AIL3
AGND	8	42	AGND
AIH2	9	43	AIL2
AIH1	10	44	AIL1
AGND	11	45	AGND
AIH0	12	46	AIL0
AO1	13	47	AGND
AO0	14	48	AGND
+12V or 5V	15	49	+12V or 5V
Ext. Time Base or GPTC CLK0	16	50	Ext. CONVSN. or GPTC CLK1
DI0 / DI0 / EA0+	17	51	DI8 / GPTC GATE0 / EA0-
DI1 / DI1 / EB0+	18	52	DI9 / GPTC GATE1 / EB0-
DI2 / DI2 / EZ0+	19	53	DI10 / AI Trigger In / EZ0-
DI3 /DI3 / EORG0+	20	54	DI11 / AO Trigger In / NA
DI4 / DI4 / NA	21	55	DI12 / NA / EORG1
DI5 / DI5 / EA1+	22	56	DI13 / NA / EA1-
DI6 / DI6 / EB1+	23	57	DI14 / NA / EB1-
DI7 / DI7 / EZ1+	24	58	DI15 / NA / EZ1-
DGND	25	59	DI Sync In
DO0	26	60	DO8 / GPTC COUT0 / DO8
DO1	27	61	DO9 / GPTC COUT1 / DO9
DO2	28	62	DO10 / NA / DO10
DO3	29	63	DO11 / NA / DO11
DO4	30	64	DO12 / NA / DO12
DO5	31	65	DO13 / NA / DO13
DO6	32	66	DO14 / NA / DO14
DO7	33	67	DO15 / NA / DO15
DGND	34	68	DO Sync Out

Figure 2-22: PCIe-9147 CN1 Pin Assignments

Signal Name	I/O	Description
AIH <0…7>	I	Differential Analog High Input Channels 0-7
AIL <0…7>	I	Differential Analog Low Input Channels 0-7
AO <0,1>	O	Analog Output Channels <0,1>
AGND		Analog Ground
Ext. Time Base	I	External Time Base Clock Signal Input
Ext. CONVSN	I	External Conversion Clock Signal Input
AI Trigger In	I	External Analog Input Trigger Signal Input
AO Trigger In	I	External Analog Output Trigger Signal Input
DI <0…15>	I	Digital Input Channels 0-15
DI Sync In	I	Digital Input synchronization clock source
DO <0…15>	O	Digital Output Channels 0-15
DO Sync Out	O	Digital Output synchronization clock source out
GPTC CLK <0,1>	I	Source clock input of GPTC<0,1>
GPTC GATE <0,1>	I	Gate Input of GPTC<0,1>
GPTC COUT <0,1>	O	Output of GPTC<0,1>
EA <0,1>	I	Encoder A Phase
EB <0,1>	I	Encoder B Phase
EZ <0,1>	I	Encoder Z Phase
EORG <0,1>	I	Encoder Original Signal
DGND		Digital Ground
+12V	O	12V power output @ 0.2A
5V	O	5V power output @ 0.2A
NC		No connect
NA		No function
AI_AO_Cal	I	Calibration Voltage Input, only factory used.

Table 2-9: PCIe-9146/9147 CN1 Pin Assignment Legend

2.4.3 PCIe-9161/9163/9164

The PCIe-9146/9147 comes equipped with one/two 68-pin SCSI-type female connector (CN1/CN6) and two 20-pin insulation displacement connectors (CN7/CN8). CN1/CN6 are located on the faceplate and CN7/CN8 are located on the board. CN1/CN6 are used for analog input/output, and CN7/CN8 are used for digital signal input/output.

2.4.3.1 PCIe-9161/9163/9164 CN1/CN6 Connector

CN1/CN6 are 68-pin SCSI-type female connectors with the following pin assignments.

NC	1	35	NC
NC	2	36	NC
NC	3	37	NC
NC	4	38	NC
AGND	5	39	AGND
AGND	6	40	AGND
AI15	7	41	NC
AI14	8	42	NC
AI13	9	43	NC
AI12	10	44	NC
AI11	11	45	NC
AI10	12	46	NC
AI9	13	47	NC
AI8	14	48	NC
AI7 / AI7+	15	49	AI7-
AI6 / AI6+	16	50	AI6-
AI5 / AI5+	17	51	AI5-
AI4 / AI4+	18	52	AI4-
AI3 / AI3+	19	53	AI3-
AI2 / AI2+	20	54	AI2-
AI1 / AI1+	21	55	AI1-
AI0 / AI0+	22	56	AI0-
AGND	23	57	AGND
NC	24	58	AGND
NC	25	59	AGND
AO1	26	60	AGND
AO0	27	61	AGND
AI_AO_Cal+	28	62	AI_AO_Cal-
AGND	29	63	AGND
NC	30	64	NC
DGND	31	65	DGND
Ext. Time Base	32	66	Ext. CONVT
AO_Trig	33	67	AI_Trig
+12V or 5V	34	68	DGND

Figure 2-23: PCIe-9161 CN1 Pin Assignments

NC	1	35	NC
NC	2	36	NC
NC	3	37	NC
NC	4	38	NC
AGND	5	39	AGND
AGND	6	40	AGND
AI15 / AI15+	7	41	AI16 / AI15-
AI14 / AI14+	8	42	AI17 / AI14-
AI13 / AI13+	9	43	AI18 / AI13-
AI12 / AI12+	10	44	AI19 / AI12-
AI11 / AI11+	11	45	AI20 / AI11-
AI10 / AI10+	12	46	AI21 / AI10-
AI9 / AI9+	13	47	AI22 / AI9-
AI8 / AI8+	14	48	AI23 / AI8-
AI7 / AI7+	15	49	AI24 / AI7-
AI6 / AI6+	16	50	AI25 / AI6-
AI5 / AI5+	17	51	AI26 / AI5-
AI4 / AI4+	18	52	AI27 / AI4-
AI3 / AI3+	19	53	AI28 / AI3-
AI2 / AI2+	20	54	AI29 / AI2-
AI1 / AI1+	21	55	AI30 / AI1-
AI0 / AI0+	22	56	AI31 / AI0-
AGND	23	57	AGND
AO3	24	58	AGND
AO2	25	59	AGND
AO1	26	60	AGND
AO0	27	61	AGND
AI_AO_Cal+	28	62	AI_AO_Cal-
AGND	29	63	AGND
NC	30	64	NC
DGND	31	65	DGND
Ext. Time Base	32	66	Ext. CONVT
AO_Trig	33	67	AI_Trig
+12V or 5V	34	68	DGND

Figure 2-24: PCIe-9163/9164 CN1 Pin Assignments

NC	1	35	NC
NC	2	36	NC
NC	3	37	NC
NC	4	38	NC
NC	5	39	NC
NC	6	40	NC
NC	7	41	NC
NC	8	42	NC
AGND	9	43	AGND
AGND	10	44	AGND
AI47 / AI31+	11	45	AI48 / AI31-
AI46 / AI30+	12	46	AI49 / AI30-
AI45 / AI29+	13	47	AI50 / AI29-
AI44 / AI28+	14	48	AI51 / AI28-
AI43 / AI27+	15	49	AI52 / AI27-
AI42 / AI26+	16	50	AI53 / AI26-
AI41 / AI25+	17	51	AI54 / AI25-
AI40 / AI24+	18	52	AI55 / AI24-
AI39 / AI23+	19	53	AI56 / AI23-
AI38 / AI22+	20	54	AI57 / AI22-
AI37 / AI21+	21	55	AI58 / AI21-
AI36 / AI20+	22	56	AI59 / AI20-
AI35 / AI19+	23	57	AI60 / AI19-
AI34 / AI18+	24	58	AI61 / AI18-
AI33 / AI17+	25	59	AI62 / AI17-
AI32 / AI16+	26	60	AI63 / AI16-
AGND	27	61	AGND
AGND	28	62	AGND
NC	29	63	NC
NC	30	64	NC
NC	31	65	NC
NC	32	66	NC
NC	33	67	NC
NC	34	68	NC

Figure 2-25: PCIe-9164 CN6 Pin Assignments

Signal Name	I/O	Description
AI+ <0…31>	I	Differential Analog High Input Channels 0-31
AI- <0…31>	I	Differential Analog Low Input Channels 0-31
AO <0,3>	O	Analog Output Channels <0,3>
AGND		Analog Ground
Ext. Time Base	I	External Time Base Clock Signal Input
Ext. CONVSN	I	External Conversion Clock Signal Input
AI Trigger In	I	External Analog Input Trigger Signal Input
AO Trigger In	I	External Analog Output Trigger Signal Input
DGND		Digital Ground
+12V	O	12V power output @ 0.2A
5V	O	5V power output @ 0.2A
NC		No connect
NA		No function
AI_AO_Cal	I	Calibration Voltage Input, only factory used.

Table 2-10: PCIe-9161/9163/9164 CN1/CN6 Pin Assignment Legend

2.4.3.2 PCIe-9161/9163/9164 CN7/CN8 Connector

CN7/CN8 are 20-pin insulation displacement connectors with the following pin assignments.

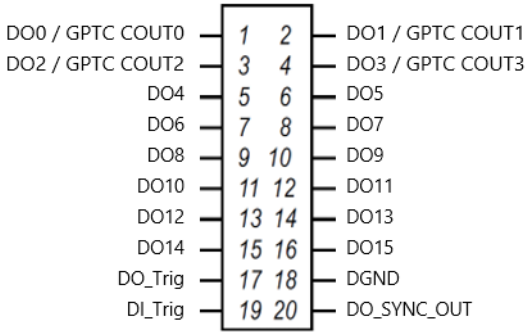


Figure 2-26: PCIe-9161/9163/9164 CN7 Pin Assignments

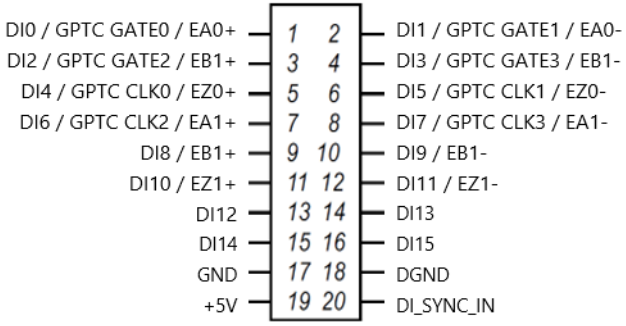


Figure 2-27: PCIe-9161/9163/9164 CN8 Pin Assignments

Signal Name	I/O	Description
AGND		Analog Ground
DI <0...15>	I	Digital Input Channels 0-15
DI Sync In	I	Digital Input Synchronization Clock Source In
DO <0...15>	O	Digital Output Channels 0-15
DO Sync Out		Digital Output Synchronization Clock Source Out
GPTC CLK <0,3>		Source Clock Input of GPTC <0,3>
GPTC Gate <0,3>		Gate Input of GPTC <0,3>
GPTC COUT <0,3>		Output of GPTC <0,3>
EA <0,1>		Encoder A Phase
EB <0,1>		Encoder B Phase
EZ <0,1>		Encoder Z Phase
DGND		Digital Ground
5V	O	5V power output @ 0.2A
NC		No connect
NA		No function

Table 2-11: PCIe-9161/9163/9164 CN7/CN8 Pin Assignment Legend

2.5 Hardware Installation Outline

2.5.1 PCI Express Configuration

PCI Express cards are equipped with a plug and play PCI Express controller that can request base addresses and interrupts according to the PCI Express standard. The system BIOS will configure resources based on the PCI Express cards' configuration registers and system parameters (set in the BIOS). Interrupt assignment and memory usage (I/O port locations) of the PCI Express cards can be assigned by the system BIOS only. These system resource assignments are done on a board-by-board basis. It is not suggested to assign the system resource by any other method.

2.5.2 PCI Express Slot Selection

A PCIe-9100 Series card can be inserted into any PCI Express slot without the need to configure system resources.

2.5.3 Installation Procedures

1. Turn off your computer.
2. Turn off all peripherals connected to your computer (printer, monitor, etc.).
3. Remove the cover from your computer.
4. Setup jumpers and switchs on the PCIe-9100 Series card.
5. Before handling PCI Express cards, discharge any static buildup on your body by touching the metal case of the computer. Hold the edge and do not touch the components.
6. Position the board into the PCI Express slot you have selected.
7. Secure the card in place at the rear panel of the system.

2.6 Device Installation for Windows Systems

Once Windows 7/10/11 or later has started, the Plug and Play function of Windows system will find the new NuDAQ cards. If this is the first time the NuDAQ cards are running on your Windows system, you will be prompted to input the device information source. Please refer to the ***Software Installation Guide*** for step-by-step installation procedures.

3 Operation Theory

This chapter describes the operation theory of the PCIe-9100 Series card functions. The functions include A/D conversion, D/A conversion, Digital I/O and counter/timer usage. The operation theory can help you to understand how to configure or to program the PCIe-9100 Series cards.

3.1 A/D Conversion

Before programming the PCIe-9100 Series card to perform any A/D conversions, you should have an understanding of the following:

- A/D front-end signal input connection
- A/D conversion procedure
- A/D trigger mode
- A/D data transfer mode
- Signal Connection
- AI data format

3.2 Analog Input Signal Connection

The PCIe-9100 Series provides single-ended or differential analog input channels. The analog signals can be converted to digital values by the A/D converter. To avoid ground loops and to obtain more accurate measurements, it is important to understand the signal source type and how to choose the analog input modes, either signal-ended or differential. The mode can be selected by software settings.

Single-ended Mode

The single-ended mode has only one input relative to ground and is suitable for connecting with a *floating signal source*. A floating source is one that does not have any connection to ground. Figure 3-1 shows the single-ended connection. Note that when more than two floating sources are available, the sources must have a common ground.

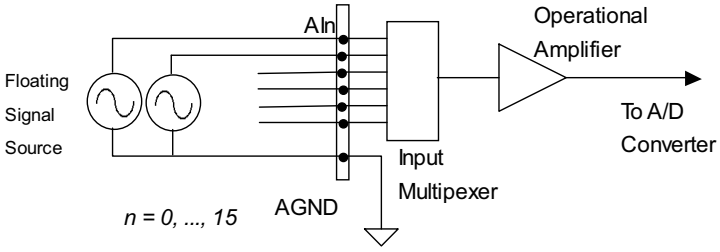


Figure 3-1: Floating source and single-ended

Differential Input Mode

The differential input mode provides two inputs that respond to differences in signals. If the signal source has one side connected to local ground, the differential mode can be used to reduce the effect of ground loops. Figure 3-2 shows the connection for differential input mode. However, if the signal source is locally grounded, the single-ended mode can be used when the Vcm (Common Mode Voltage) is very small and the effect of ground loops is minimal.

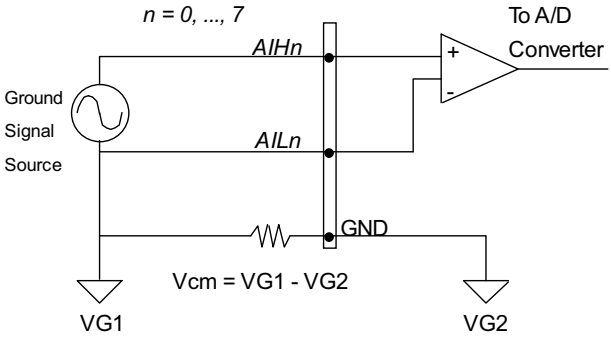


Figure 3-2: Ground source and differential input

A differential mode must be used when the signal source is differential. A differential source means that the ends of the signal are not grounded. To avoid the danger of high voltages between the local ground of the signal and the ground of the PC system, a shorted ground path must be connected. Figure 3-3 shows the connection for a differential source.

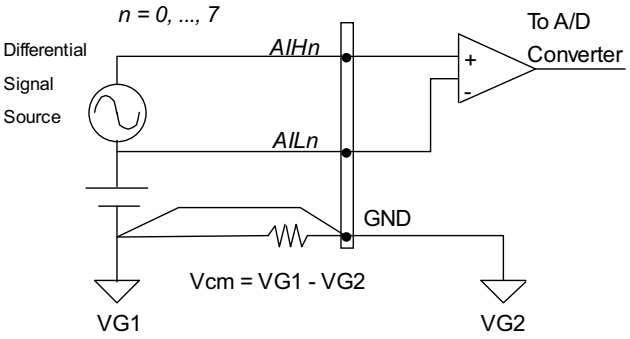


Figure 3-3: Differential source and differential input

If the signal source are both floating, you should use the differential mode, and the floating signal source should be connected as in Figure 3-4.

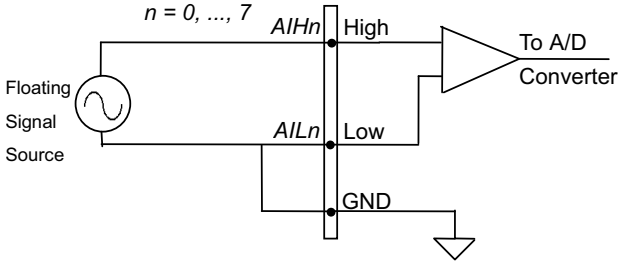


Figure 3-4: Floating source and differential input

3.2.1 A/D Conversion Procedure

A/D conversion starts when a trigger is set by the trigger source. The PCIe-9100 Series provides three trigger modes. See section 3.2.2.

The A/D data should now be transferred into the PC's memory for further processing. The PCIe-9100 Series provides three data transfer modes that allow users to optimize the DAQ system. See section for data transfer modes.

3.2.2 A/D Trigger Sources

A/D conversion can be triggered by an *Internal* or *External* trigger source. Whenever an external source is set, the internal sources are disabled.

Totally there are three trigger sources available to the PCIe-9100 Series. The different trigger conditions are specified below.

Software Trigger

This trigger source is software controllable. That is, the A/D conversion starts when any value is written into the software trigger register. This trigger mode is suitable for low speed A/D conversions. Under this mode, the timing of the A/D conversion is fully controlled by the software. However, it is difficult to control a fixed A/D conversion rate unless another timer interrupt service routine is used to generate a fixed rate trigger.

External Digital Trigger

Through Pin ExtTrig, an external digital trigger is generated when a TTL rising edge or falling edge is detected. The trigger polarity can be selected by software. Note that the signal level of the external digital trigger signal should be TTL compatible, and the minimum pulse width 50 ns.

Analog Trigger

From any channel selected as an analog trigger source for A/D conversion, FPGA could generate a trigger signal when the analog trigger condition is satisfied. The PCIe-9100 Series uses two threshold voltages, Low_Threshold and High_Threshold, to build five different trigger conditions that are software configurable.

Below-Low analog trigger condition

Figure 3-5 shows the below-low analog trigger condition. The trigger signal is generated when the input analog signal is less than the Low_Threshold voltage. The High_Threshold setting is not used in this trigger condition.

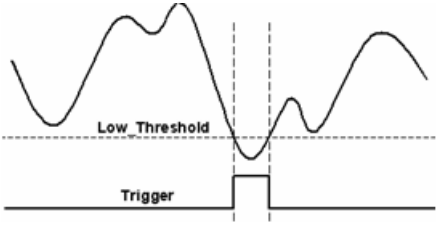


Figure 3-5: Below-Low analog trigger condition

Above-High analog trigger condition

Figure 3-6 shows the above-high analog trigger condition. The trigger signal is generated when the input analog signal is higher than the High_Threshold voltage. The Low_Threshold setting is not used in this trigger condition.

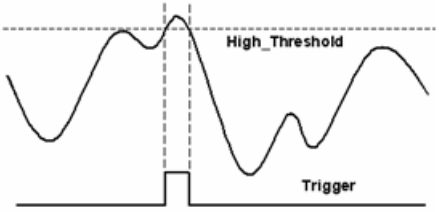


Figure 3-6: Above-High analog trigger condition

Inside-Region analog trigger condition

Figure 3-7 shows the inside-region analog trigger condition. The trigger signal is generated when the input analog signal level falls in the range between the High_Threshold and the Low_Threshold voltages.

NOTE: The High_Threshold setting should be always higher than the Low_Threshold voltage setting.

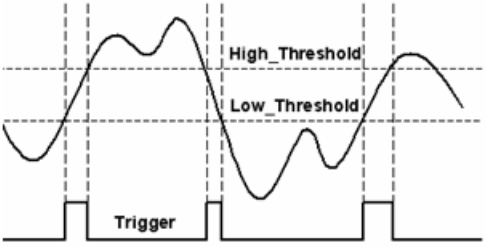


Figure 3-7: Inside-Region analog trigger condition

High-Hysteresis analog trigger condition

Figure 3-8 shows the high-hysteresis analog trigger condition. The input analog signal level should be greater than the Low_Threshold voltage at first, and then the trigger signal will be generated when the input analog signal level is greater than High_Threshold voltage to determine the hysteresis duration.

NOTE:

The High_Threshold setting should be always higher than the Low_Threshold voltage setting.

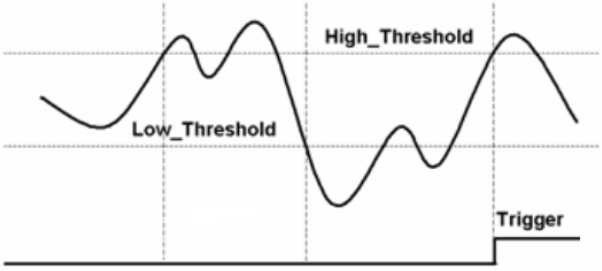


Figure 3-8: High-Hysteresis analog trigger condition

Low-Hysteresis analog trigger condition

Figure 3-9 shows the low-hysteresis analog trigger condition. The input analog signal level should be lower than the High_Threshold voltage at first, and then the trigger signal will be generated when the input analog signal level is lower than Low_Threshold voltage to determine the hysteresis duration.

NOTE:

The High_Threshold setting should be always higher than the Low_Threshold voltage setting.

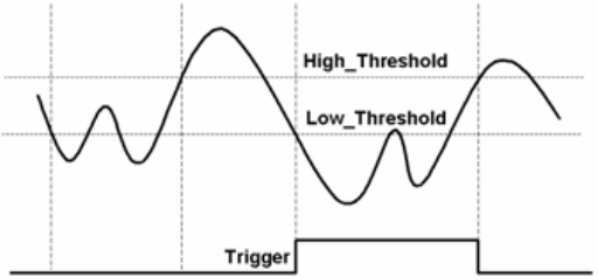


Figure 3-9: Low-Hysteresis analog trigger condition

3.2.3 A/D Trigger Modes

There are 4 trigger modes (pre-trigger, post-trigger, middle-trigger, delay-trigger, post-trigger with re-trigger and delay-trigger with re-trigger) working with the 3 trigger sources to initiate different scan data acquisition timing when a trigger event occurs.

Pre-Trigger Acquisition

Use pre-trigger acquisition in applications where you want to collect data before a trigger event. The A/D starts to sample when you execute the specified function calls to begin the pre-trigger operation, and stops when the trigger event occurs. Users must program the value M in M_counter to specify the amount of the stored scans before the trigger event. If an external trigger occurs, the program only stores the last M scans of data converted before the trigger event, as illustrated in Figure 3-10, where M_counter = M =3, PSC_counter = 0. The post scan count is 0 because there is no sampling after the trigger event in pre-trigger acquisition. The total stored amount of data = Number of enabled channels * M_counter.

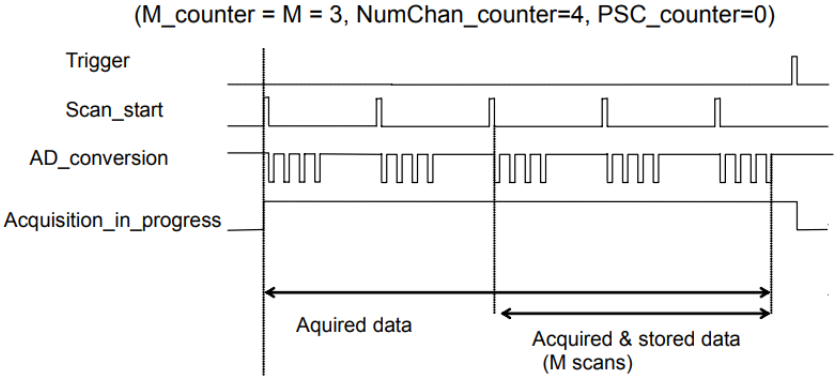


Figure 3-10: Pre-trigger (trigger occurs after at least M scans acquired)

If a trigger event occurs when a scan is in progress, the data acquisition will not stop until the scan completes, and the stored M scans of data includes the last scan. Therefore, the first stored data will always be the first channel entry of a scan (that is, the first channel entry in the Channel Gain Queue if the number of entries in the Channel Gain Queue is equivalent to the value of NumChan_counter), no matter when a trigger signal occurs, as illustrated in Figure 3-11, where
M_counter = M = 3, NumChan_counter = 4, PSC_counter = 0.

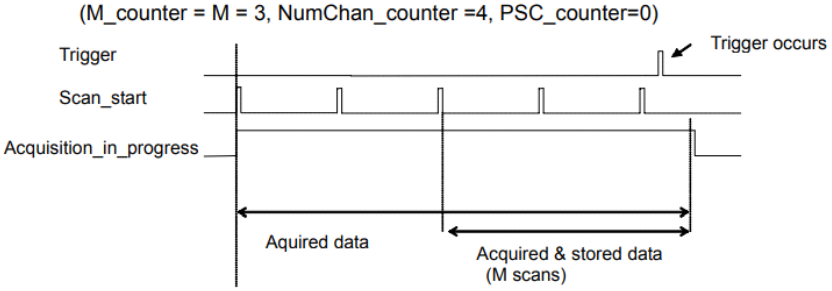


Figure 3-11: Pre-trigger (Trigger with scan in progress)

When the trigger signal occurs before the first M scans of data are converted, the amount of stored data could be fewer than the originally specified amount in M_counter, as illustrated in Figure 3-12. This situation can be avoided by setting M_enable. If M_enable is set to 1, the trigger signal will be ignored until the first M scans of data are converted, and it assures the user M scans of data under pre-trigger mode, as illustrated in Figure 3-13. However, if M_enable is set to 0, the trigger signal will be accepted any time, as shown in Figure 3-12. Note that the total amount of stored data will always be equal to the number in the M_counter because data acquisition does not stop until a scan is completed.

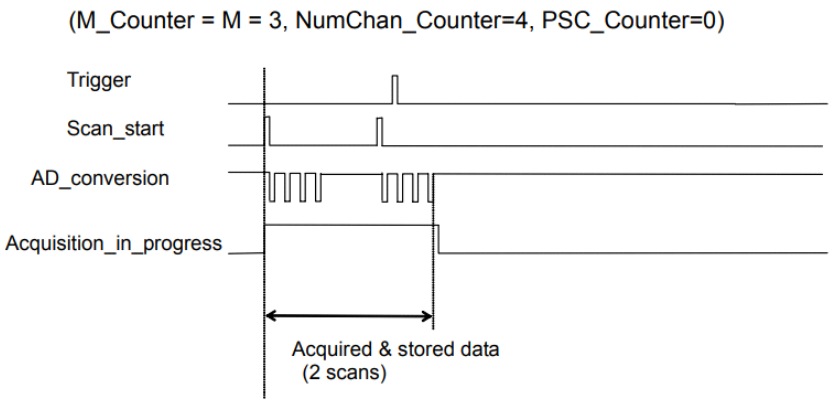
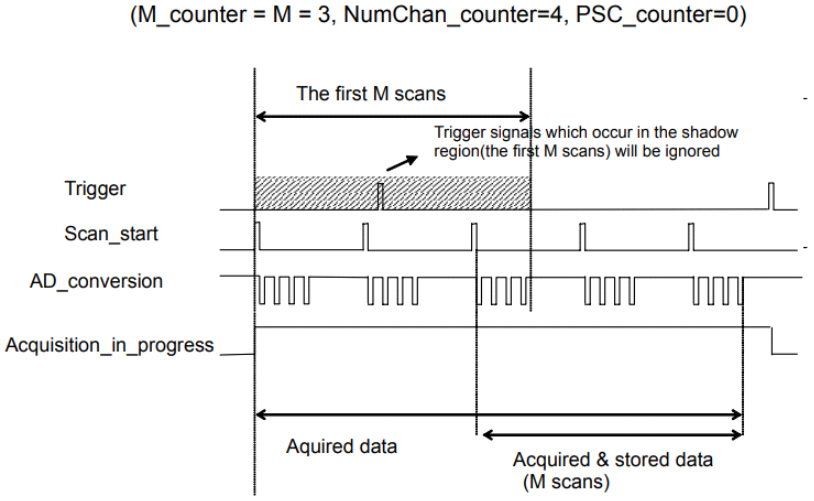


Figure 3-12: Pre-trigger with M_enable=0 (Trigger occurs before M scans)



[Max. value of M_counter is 65536]

Figure 3-13: Pre-trigger with M_enable=1

Middle-Trigger Acquisition

Use middle-trigger acquisition in applications where you want to collect data before and after a trigger event. The number of scans (M) stored before the trigger is specified in M_counter, while the number of scans (N) after the trigger is specified in PSC_counter. Like pre-trigger mode, the number of stored data could be less than the specified amount of data (M+N), if an external trigger occurs before M scans of data are converted. The M_enable bit in middle-trigger mode takes the same effect as in pre-trigger mode. If M_enable is set to 1, the trigger signal will be ignored until the first M scans of data are converted, and it assures the user with (M+N) scans of data under middle-trigger mode. However, if M_enable is set to 0, the trigger signal will be accepted at any time. Figure 3-14 shows the acquisition timing with M_enable=1.

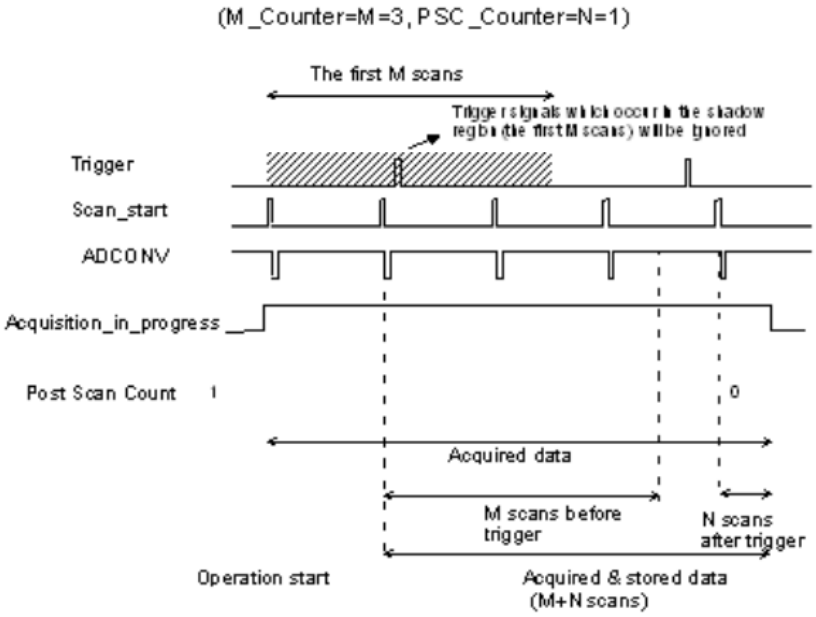


Figure 3-14: Middle trigger with M_enable = 1

If the trigger event occurs when a scan is in progress, the stored N scans of data would include this scan, as illustrated in Figure 3-15.

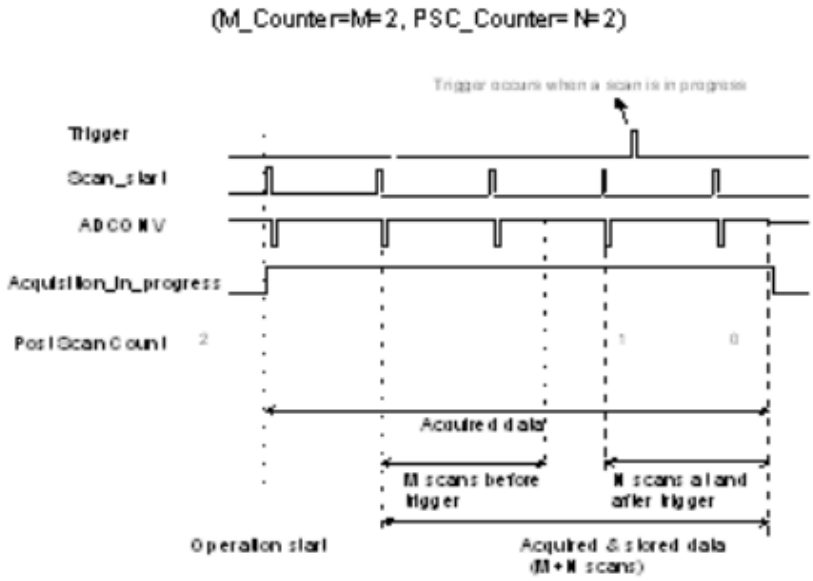


Figure 3-15: Middle trigger (trigger occurs when a scan is in progress)

NOTE:

M_counter defined in Middle-Trigger is different from that of Pre-Trigger. In Middle-trigger, M_Counter ends counting before the trigger event while in Pre-Trigger, M_Counter ends counting right at or before a trigger event. Refer to Figure 3-14 and Figure 3-15.

Post-Trigger Acquisition

Use post-trigger acquisition in applications where you want to collect data after a trigger event. The number of scans after the trigger is specified in PSC_counter, as illustrated in Figure 3-16. The total acquired data length = number of enable-channel * PSC_counter.

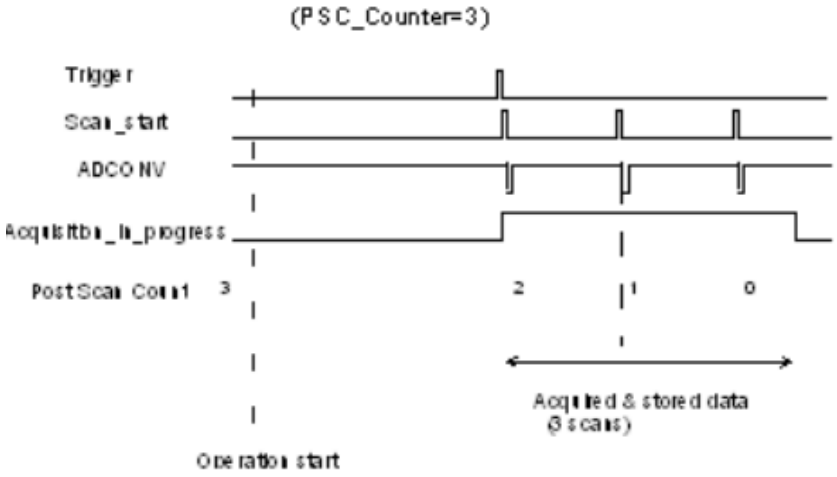


Figure 3-16: Post trigger

Delay-Trigger Acquisition

Use delay trigger acquisition in applications where you want to delay the data collection after the occurrence of a specified trigger event. The delay time/samples are controlled by the value, which is pre-loaded in the Delay_counter (16-bit). The counter counts down on the rising edge of the Delay_counter clock source after the trigger condition is met. The clock source can be software programmed either by the TIMEBASE clock (64MHz) or A/D sampling clock (TIMEBASE / SI_counter). When the count reaches 0, the counter stops and the card starts to acquire data. The total acquired data length = number of enable-channel * PSC_counter.

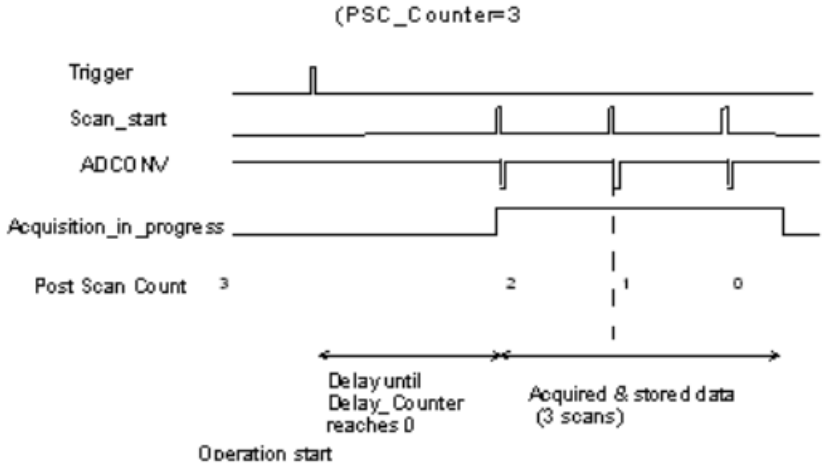


Figure 3-17: Delay trigger

NOTE:

When the Delay_counter clock source is set to TIMEBASE, the maximum delay time = 2^32/64M s = 67Sec, and when the source is set to A/D sampling clock, the maximum delay time can be as high as (2^32 * SI_counter / 64M).

Post-Trigger or Delay-Trigger Acquisition with Re-trigger

Use post-trigger or delay-trigger acquisition with the re-trigger function in applications where you want to collect data after several trigger events. The number of scans after each trigger is specified in PSC_counter, and users can program Retrig_no to specify the number of re-triggers. Figure 3-18 illustrates 2 scans of data acquired after the first trigger signal, then the card waits for the re-trigger signal. Re-trigger signals which occur before the first 2 scans are completed will be ignored. When the re-trigger signal occurs, 2 more scan are performed. The process repeats until the specified amount of re-trigger signals are detected. The total acquired data length = number of enable-channel * PSC_counter * Retrig_no.

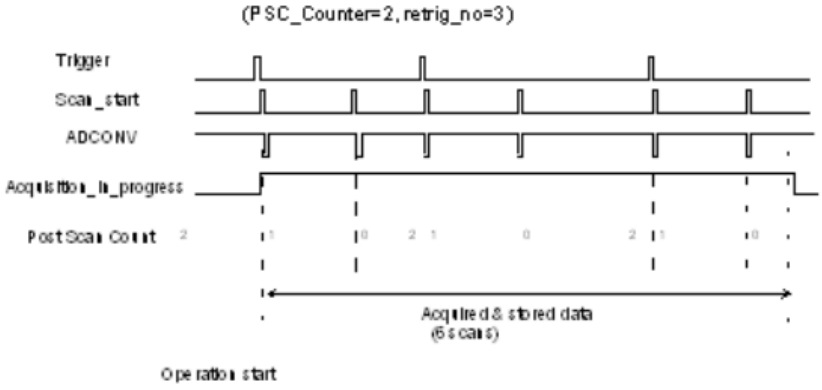


Figure 3-18: Post trigger with re-trigger

3.2.4 A/D Data Transfer Modes

Any of the two A/D data transfer modes can be used when a conversion is completed. The Data Transfer Mode is controlled by the A/D mode control bits of the A/D control register. The different transfer modes are specified below.

Software Data Transfer

Usually, this mode is used with software A/D trigger mode. The conversion starts when it receives a software trigger, the software then polls the *DRDY* bit on the A/D Status register until it becomes high. When it is low, the A/D data is read, and the *DRDY* bit will be cleared to indicate the data transfer is completed.

It is possible to read A/D converted data without polling. The A/D conversion time takes no more then 1μs on the PCIe-9100 Series card. Hence, after a software trigger, the software can wait for at least 1μs then read the A/D register without polling.

DMA Transfer

The DMA (Direct Memory Access) bus master allows data to be transferred directly between the PCIe-9100 Series and the PC's memory at the fastest possible rate, without using up any CPU time. The A/D data is queued in the local FIFO on the PCIe-9100 Series itself and it is automatically transferred to PC's memory.

The DMA transfer mode is very complex to program. It is recommended to use high-level programming libraries to operate this card. If you wish to program software to handle the DMA bus master data transfer, refer to the PCI Express controller manual for more details.

3.2.5 AI Data Format

The data format of the acquired 16- and 14-bit A/D data is 2's complement coding. Table 3-1 and Table 3-2 show the valid input ranges and the ideal transfer characteristics.

Description	Bipolar Analog Input Range						Digital Code (16-bit)
Full-scale Range	±10V	±5V	±2.5V	±1.25V	±0.625V	±0.3125V	
Least significant bit	305.2uV	152.6uV	76.3uV	38.14uV	19.07uV	9.54uV	
FSR-1LSB	9.999695V	4.999847V	2.499924V	1.249961V	0.624981V	0.31249V	7FFF
Midscale +1LSB	305.2uV	152.6uV	76.3uV	38.14uV	19.07uV	9.54uV	0001
Midscale	0V	0V	0V	0V	0V	0V	0000
Midscale -1LSB	-305.2uV	-152.6uV	-76.3uV	-38.14uV	-19.07uV	-9.54uV	FFFF
-FSR	-10V	-5V	-2.5V	-1.25V	-0.625V	-0.3125V	8000

Table 3-1: Bipolar Analog Input Range and Output Digital Code (16-bit)

Description	Bipolar Analog Input Range						Digital Code (14-bit)
Full-scale Range	±10	±5	±2.5	±1.25	±0.625	±0.3125	
Least significant bit	1220.7uV	610.4uV	305.2uV	152.6uV	76.3uV	38.1uV	
FSR-1LSB	9.9987793V	4.9993896V	2.4996948V	1.2498474V	0.6249237V	0.3124619V	1FFF
MID+1LSB	1220.7uV	610.4uV	305.2uV	152.6uV	76.3uV	38.1uV	0001
MID	0V	0V	0V	0V	0V	0V	0000
MID-1LSB	-1220.7uV	-610.4uV	-305.2uV	-152.6uV	-76.3uV	-38.1uV	3FFF
-FSR	-10V	-5V	-2.5V	-1.25V	-0.625V	-0.3125V	2000

Table 3-2: Bipolar Analog Input Range and Output Digital Code (14-bit)

3.3 D/A Conversion

For complex applications, the PCIe-9100 Series offer software polling to update the output, and DMA data transfer to generate waveforms. This means that the D/A update rate is not only controlled by software timing, but can also be set by a precision hardware timer that is user specified. The following sections discuss the PCIe-9100 Series D/A architecture and control methods.

Definition	Pin No,		Definition
	1	20	
	...	...	
	9	27	
	10	28	
AGND	11	29	AGND
	12	30	AO1
	13	31	
	14	32	AO2
DGND	15	33	
	16	34	
Ext Trg	17	35	
	18	36	
	19	37	Ext CLK

Table 3-3: PCIe-9101/9121/9141 Analog Output Mode on CN3 Pin Assignments

Definition	Pin No,		Definition
	1	35	
	...	...	
	12	46	
AO1	13	47	AGND
AO0	14	48	AGND
	15	49	
Ext. Time Base	16	50	
	...	...	
	19	53	
	20	54	AO Trigger In
	21	55	
	...	...	
DGND	34	68	

Table 3-4: PCIe-9146/9147 Analog Output Mode on CN1 Pin Assignments

Definition	Pin No,		Definition
	1	35	
	...	...	
	22	56	
AGND	23	57	AGND
	24	58	
	25	59	
AO1	26	60	
AO0	27	61	
	28	62	
	...	...	
DGND	31	65	DGND
	32	66	
AO Trigger	33	67	
	34	68	

Table 3-5: PCIe-9161 Analog Output Mode on CN1 Pin Assignments

Definition	Pin No,		Definition
	1	35	
	...	...	
	22	56	
AGND	23	57	AGND
AO3	24	58	
AO2	25	59	
AO1	26	60	
AO0	27	61	
	28	62	
	...	...	
DGND	31	65	DGND
	32	66	
AO Trigger	33	67	
	34	68	

Table 3-6: PCIe-9163/9164 Analog Output Mode on CN1 Pin Assignments

3.3.1 Bipolar Output Modes

The PCIe-9100 Series series supports a maximum ±10 V voltage output. Table 3-7 illustrates the relationship of straight binary coding between the digital codes and output voltages.

Digital Code	Analog Output
0x7FFF	9.9997V
0x4000	5V
0x0000	0V
0xC000	-5V
0x8000	-10V

Table 3-7: Bipolar Output Codes

3.3.2 Software Update

This method is suitable for applications that need to generate D/A output controlled by user programs. In this mode, the D/A converter generates one output once the software command is issued. However, it is difficult to determine the software update rate under a multitasking OS such as Windows.

3.3.3 Waveform Generation

Waveform Generation Data Structure

FIFO is a hardware first-in first-out data queue that holds temporary digital codes for D/A conversion. When a PCIe-9100 Series operates in waveform generation mode, the waveform patterns are stored in FIFO with 1024 samples (shared).

Waveform patterns larger than 1024 samples are also supported using bus-mastering DMA transfer via the PCIe controller. Data format in FIFO is shown in Figure 3-19.

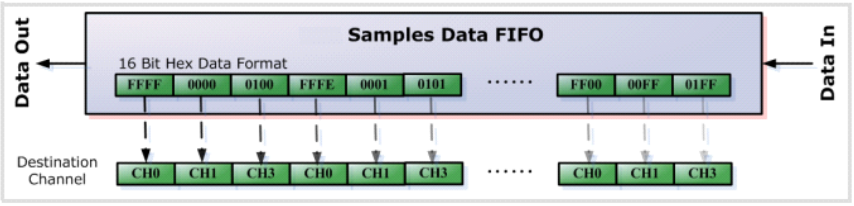


Figure 3-19: FIFO Data In/Out Structure

With hardware-based waveform generation, D/A conversions are updated automatically by the FPGA rather than by the application software. Compared with conventional software based waveform generation, the precise hardware timing control guarantees non-distorted waveform generation even when the host CPU is under heavy loading.

Waveform Generation Clock Source

When the onboard DAC receives a conversion clock signal, it will trigger a D/A update. The update clock of PCIe-9100 Series may come from two different clock sources: internal hardware timer, or external timebase clock source (CN3 pin 37). You can choose the update clock source by setting the AO source configuration

Waveform Generation with Internal Hardware Timer

Six counters interact with the waveform to generate different DAWR timings to form various waveforms. These are described in Table 3-8 and illustrated in Figure 3-20.

Counter Name	Width	Description	Note
UI_counter	32-bit	**Update Interval.** Defines the update interval between each data output.	Update Interval = Timebase* / UI_counter
UC_counter	32-bit	**Update Counts.** Defines the number of data in a waveform.	When value in UC_counter is smaller than the size of waveform patterns, the waveform is generated piece-wisely.
IC_counter	32-bit	**Iteration Counts.** Defines how many times the waveform is generated.	
Trig_counter	32-bit	Defines the acceptable start trigger count when re-trigger function is enabled	

Table 3-8: Summary of Counters for Waveform Generation

NOTE:

- Timebase = 64M Hz
- The maximum D/A update rate is 1 MHz, and the minimum UI_counter setting is 64.

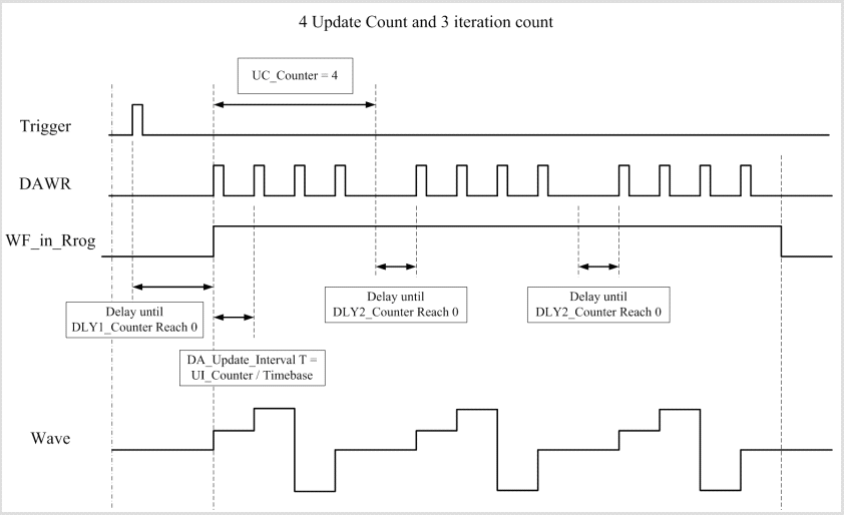


Figure 3-20: Typical D/A Timing of Waveform Generation

3.3.4 Trigger Modes

Post-Trigger Generation

Use post-trigger generation when you want to generate a waveform right after a trigger signal. The number of patterns to be updated after the trigger signal is specified by UC_counter* IC_counter, illustrated in Figure 3-21.

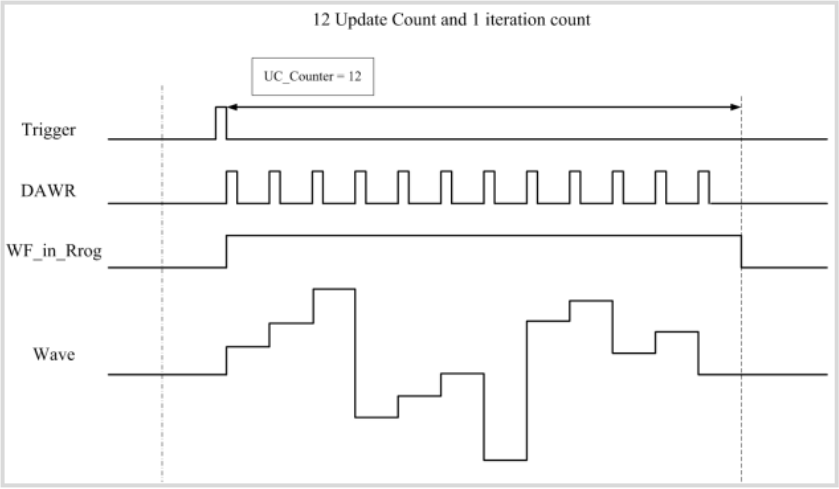


Figure 3-21: Post-Trigger Generation

Post-Trigger with Retrigger

Use post-trigger with retrigger to generate multiple waveforms with respect to multiple incoming trigger signals. Set Trig_counter to specify the number of acceptable trigger signals. Figure 3-22 Iillustrates two waveforms generated after the first trigger signal. The card then waits for another trigger signal. When the next trigger signal is asserted, the card generates two more waveforms. After two trigger signals, as specified in Trig_Counter, no more triggers signals will be accepted unless the trigger reset command is executed. For more information on Iterative Waveform Generation used in this example, refer to the next section.

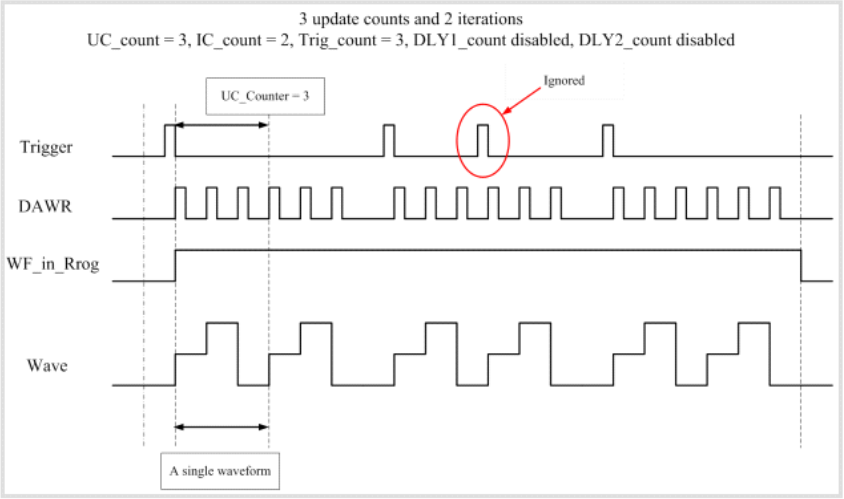


Figure 3-22: Post-Trigger with Retrigger Generation

NOTE: Start Trigger signals asserted during the waveform generation process will be ignored.

Iterative Waveform Generation

You can set the IC_counter to generate iterative waveforms regardless of the trigger mode used. The IC_counter stores the iteration number. Examples are shown in Figure 3-23 and Figure 3-24.

NOTE:

When IC_counter is disabled, the waveform generation will not stop until a stop trigger is asserted.

An onboard data FIFO is used to buffer the waveform patterns for waveform generation. If the size of a single waveform is smaller than that of the FIFO, after initially loading the data from the host computer's memory, the data in FIFO will be reused when a single waveform generation is completed and will not occupy the PCI Express bandwidth afterwards. However, if the size of a single waveform is larger than that of the FIFO, it needs to be intermittently loaded from the host computer's memory via DMA, and will occupy the PCI Express bandwidth.

If the value specified in UC_counter is smaller than the sample size of the waveform patterns, the waveform will be generated in a series of iterations. For example, if you defined a 16-sample sine wave and set the UC_counter to 2, the generated waveform will be a 1/8-cycle sine wave for every waveform period, and a complete sine wave will be generated for every 8-iterations. If you specified a UC_counter value that is larger than the sample size of the waveform LUT (for example, 32), the generated waveform will be a 2-cycle sine wave for every waveform period.

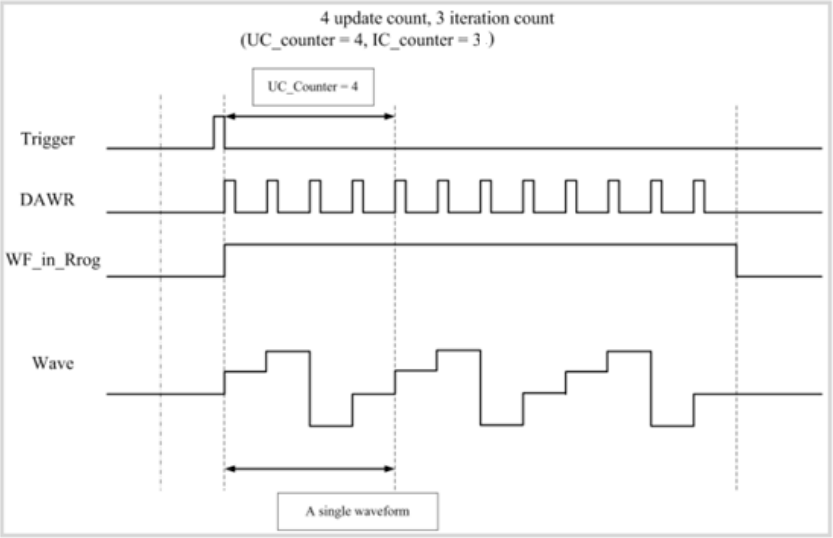


Figure 3-23: Finite Iterative Waveform Generation with Post-trigger

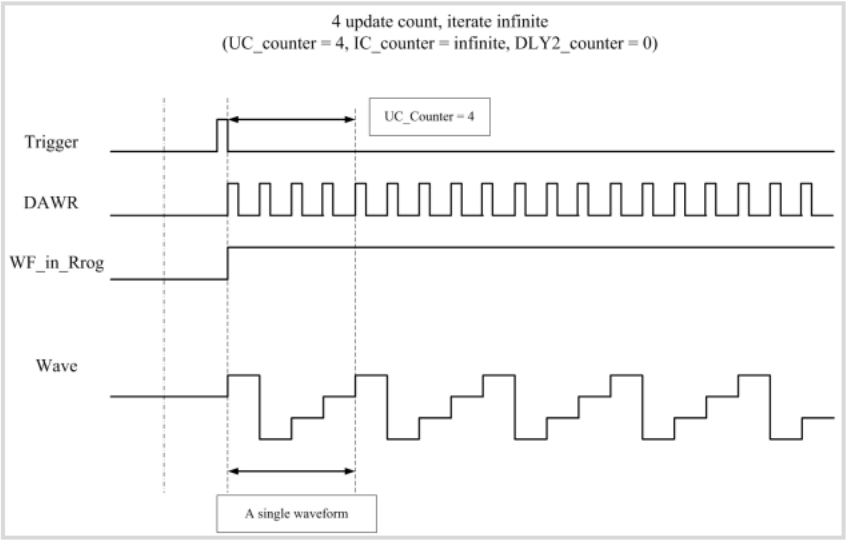


Figure 3-24: Infinite Iterative Waveform Generation with Post-trigger

3.4 Digital Input and Output

Definition	Pin No,		Definition
DI0	1	2	DI1
DI2	3	4	DI3
DI4	5	6	DI5
DI6	7	8	DI7
DI8	9	10	DI9
DI10	11	12	DI11
DI12	13	14	DI13
DI14	15	16	DI15
GND	17	18	GND
+5V	19	20	DI_SYNC_IN

Table 3-9: PCIe-9101/9121/9141 DIO Mode Pin Assignments on CN1

Definition	Pin No,		Definition
DO0	1	2	DO1
DO2	3	4	DO3
DO4	5	6	DO5
DO6	7	8	DO7
DO8	9	10	DO9
DO10	11	12	DO11
DO12	13	14	DO13
DO14	15	16	DO15
GND	17	18	GND
+5V	19	20	DI_SYNC_OUT

Table 3-10: PCIe-9101/9121/9141 DIO Mode Pin Assignments on CN2

Definition	Pin No,		Definition
	1	35	
	...	...	
DI0	17	51	DI8
DI1	18	52	DI9
DI2	19	53	DI10
DI3	20	54	DI11
DI4	21	55	DI12
DI5	22	56	DI13
DI6	23	57	DI14
DI7	24	58	DI15
DGND	25	59	
DO0	26	60	DO8
DO1	27	61	DO9
DO2	28	62	DO10
DO3	29	63	DO11
DO4	30	64	DO12
DO5	31	65	DO13
DO6	32	66	DO14
DO7	33	67	DO15
DGND	34	68	

Table 3-11: PCIe-9146/9147 DIO Mode Pin Assignments on CN1

Definition	Pin No,		Definition
DO0	1	2	DO1
DO2	3	4	DO3
DO4	5	6	DO5
DO6	7	8	DO7
DO8	9	10	DO9
DO10	11	12	DO11
DO12	13	14	DO13
DO14	15	16	DO15
DO_Trig	17	18	GND
DI_Trig	19	20	DI_SYNC_OUT

Table 3-12: PCIe-9161/9163/9164 DIO Mode Pin Assignments on CN7

Definition	Pin No,		Definition
DI0	1	2	DI1
DI2	3	4	DI3
DI4	5	6	DI5
DI6	7	8	DI7
DI8	9	10	DI9
DI10	11	12	DI11
DI12	13	14	DI13
DI14	15	16	DI15
DI16	17	18	DGND
+5V	19	20	DI_SYNC_IN

Table 3-13: PCIe-9161/9163/9164 DIO Mode Pin Assignments on CN8

3.4.1 TTL Compatible

The PCIe-9100 Series provides 16 digital input and 16 digital output channels through the connectors CN1 and CN2 on-board. The digital I/O signal is fully TTL/DTL compatible. The digital I/O signals are illustrated in Figure 3-25.

To program the digital I/O operation is fairly straightforward. The digital input operation is used to read data from corresponding registers, and the digital output operation is to write data to the corresponding registers. Note that the DIO data channel can only be read or written to in groups of 16 bits. It is impossible to access individual bits.

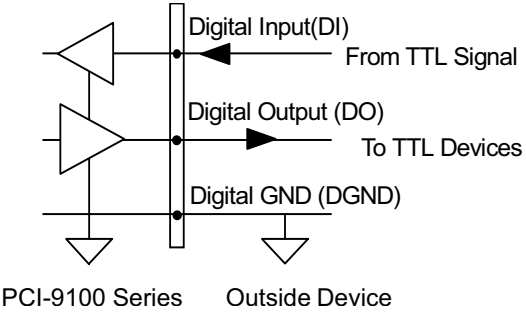


Figure 3-25: Digital I/O Connection

The PCIe-9100 Series also provides a DMA high speed data transfer mode up to 1M Hz with DI_SYNC_IN and DO_SYNC_OUT pins to synchronize DI and DO clock during data transmission.

3.4.2 Isolation (PCIe-9103 only)

Definition	Pin No,		Definition
DI0	1	2	DI1
DI2	3	4	DI3
DI4	5	6	DI5
DI6	7	8	DI7
DI8	9	10	DI9
DI10	11	12	DI11
DI12	13	14	DI13
DI14	15	16	DI15
EICOM1	17	18	EICOM2
EICOM3	19	20	EICOM4

Table 3-14: PCIe-9103 DIO Mode Pin Assignments on CN1

Definition	Pin No,		Definition
DO0	1	2	DO1
DO2	3	4	DO3
DO4	5	6	DO5
DO6	7	8	DO7
DO8	9	10	DO9
DO10	11	12	DO11
DO12	13	14	DO13
DO14	15	16	DO15
EOGND	17	18	EOGND
Vpower	19	20	Vpower

Table 3-15: PCIe-9103 DIO Mode Pin Assignments on CN2

3.4.2.1 Isolated Digital Input

There are 16 Isolated Digital input signals. Each digital input signal is connect to a photo isolator such that the signal is isolated from the ground or the power plane of the host PC. The figure below illustrates a single digital input circuit.

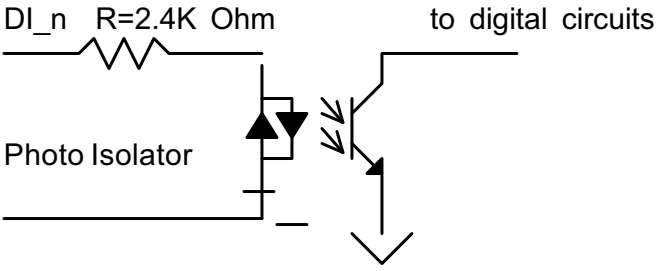


Figure 3-26: Isolated Input Circuits

The Isolated Digital input could be an AC input. The isolation voltage is 2.5KVrms. The input resistance is 2.4K ohms.

Note that the 16 DI signals are partitioned into 4 groups. Each group is based on a common plane. Every group is mutually isolated. Refer to Figure 3-27 and Table 3-16 for the four groups.

Signal Names	Common Signal
ID_0 to ID_3	EICOM1
ID_4 to ID_7	EICOM2
ID_8 to ID_11	EICOM3
ID_12 to ID_15	EICOM4

Table 3-16: Digital input signals and ground plane

The common plane could be either common power or common ground. The following diagram shows the EICOM as common ground. An external device or circuit will provide the power source or current source.

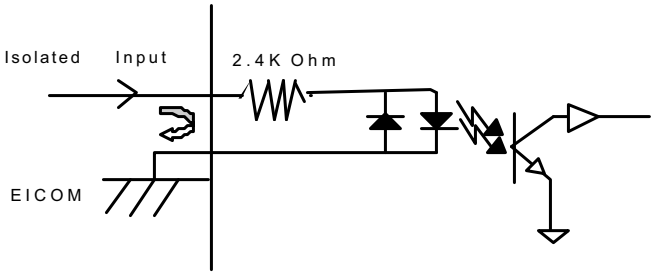


Figure 3-27: Common Ground

The following diagram shows the EICOM as common power. An external device or circuit will provide the power source and current sink. Most open collector output devices can be connected to the PCIe-9103 using this configuration.

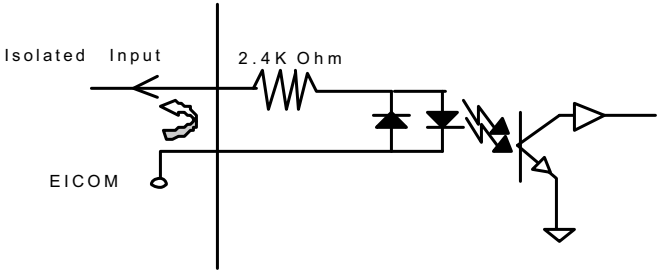


Figure 3-28: Common Power

3.4.2.2 Isolated Digital Output

There are 16 Isolated Digital output signals. Darlington transistors drive the digital output signals. Figure 3-29 shows the output circuits.

Note that the 16 DO signals uses a common ground and common external power source.

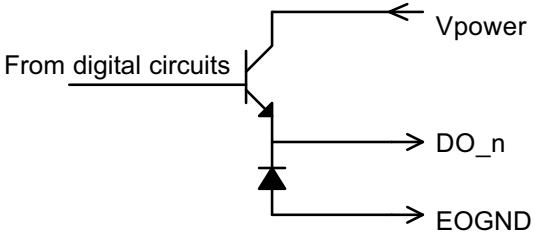


Figure 3-29: Digital Output Circuits

The EOGND pin is used via a (fly-wheel) diode. This will protect the driver if an inductive load from a relay, motor or solenoid is present. If the loading is resistive such as from resistors or LEDs, the connection to the fly-wheel diode is not necessary.

The first step in connecting the output to an external device is to distinguish the type of load. For example, if the load is a LED or a resistor, connection diagram below can be used.

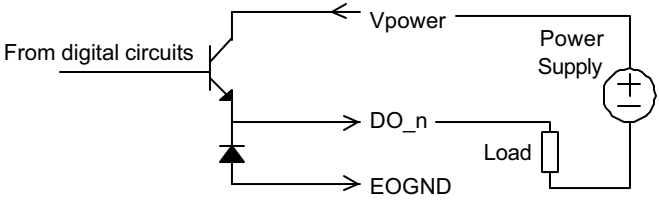


Figure 3-30: Opto-isolated output circuit for resistive loads

If the load is inductive such as from a relay, the diagram below can be used. The power supply must be from an external source in order to form a fly-wheel current loop.

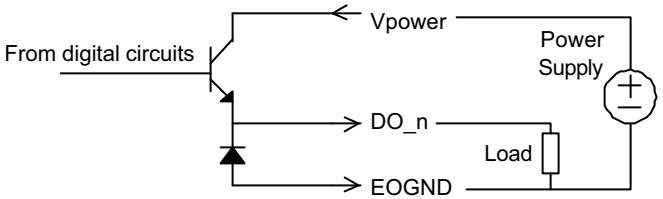


Figure 3-31: Opto-isolated output circuit for inductive loads

3.5 General Purpose Timer/Counter

The PCIe-9100 Series comes with up to four general purpose timer/counter sets featuring:

- Count up/down controlled by hardware or software
- Programmable counter clock source (internal clock up to 33 MHz, external clock up to 8 MHz)
- Programmable gate selection (hardware or software control)
- Programmable input and output signal polarities (high active or low active)
- Initial count can be loaded from a software application
- Current count value can be read back by software without affecting circuit operation
- PWM with COF (change on the fly) support

Definition	Pin No,		Definition
	1	20	
	...	...	
	14	32	
DGND	15	33	GPYC GATE0
GTPC COUT0	16	34	GPYC GATE1
	17	35	GTPC COUT1
	18	36	
	19	37	GPTC CLK

Table 3-17: PCIe-9101/9121/9141 GPTC Mode Pin Assignments on CN3

Definition	Pin No,		Definition
GPTC CLK	1	2	
GPTC COUT	3	4	
GPTC GATE	5	6	
GND	7	8	
	9	10	

Table 3-18: PCIe-9103 GPTC Mode Pin Assignments on CN4

Definition	Pin No,		Definition
	1	35	
	...	...	
GPTC CLK0	17	51	GPTC CLK1
	18	52	GPTC GATE0
	19	53	GPTC GATE1
	20	54	
	21	55	
	22	56	
	23	57	
	24	58	
	25	59	
	26	60	GPTC COUT0
	27	61	GPTC COUT1
	28	62	
	29	63	
	30	64	
	31	65	
	32	66	
	33	67	
DGND	34	68	

Table 3-19: PCIe-9146/9147 GPTC Mode Pin Assignments on CN1

Definition	Pin No,		Definition
GPTC_COUT0	1	2	GPTC_COUT1
GPTC_COUT2	3	4	GPTC_COUT3
	5	6	
	...	...	
	15	16	
	17	18	DGND
	19	20	

Table 3-20: PCIe-9161/9163/9164 GPTC Mode Pin Assignments on CN7

Definition	Pin No,		Definition
GPTC_GATE0	1	2	GPTC_GATE1
GPTC_GATE2	3	4	GPTC_GATE3
GPTC_CLK0	5	6	GPTC_CLK1
GPTC_CLK2	7	8	GPTC_CLK3
	9	10	
	...	...	
	17	18	DGND
	19	20	

Table 3-21: PCIe-9161/9163/9164 GPTC Mode Pin Assignments on CN8

3.5.1 Basic Timer/Counter Functions

Each timer/counter has three inputs that can be controlled via hardware or software applications: clock input (GPTC_CLK), gate input (GPTC_GATE), and up/down control input (GPTC_UD). The GPTC_CLK input provides a clock source input to the timer/counter controlled by software which can switch the clock source internally or externally. Active edges on the GPTC_CLK input make the counter increment or decrement. The GPTC_UD input controls the counter up or down (high: count up; low: count down), while the GPTC_GATE input is a control signal which acts as a counter enabling or a counter trigger signal under different applications. GPTC_OUT will then generate a pulse signal based on which timer/counter mode you have set. All input/output signal polarities can be programmed by software. For brevity, all GPTC_CLK, GPTC_GATE, and GPTC_OUT in the following illustrations are assumed to be active high or rising-edge triggered.

3.5.2 General Purpose Timer/Counter Modes

Eight programmable timer/counter modes are provided. All modes start operating following a software-start signal that is set by software. The GPTC software reset initializes the status of the counter and reloads the initial value to the counter. The operation remains halted until software-start is executed again. The operating theories under different modes are described in the following sections.

Mode 1: Simple Gated-Event Counting

In this mode, the counter counts the number of pulses on the GPTC_CLK after software-start. Initial count can be loaded from software. The current count value can be read back by software any time with no effect on the counting. GPTC_GATE is used to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 3-32 illustrates the operation with initial count = 5, count-down mode.

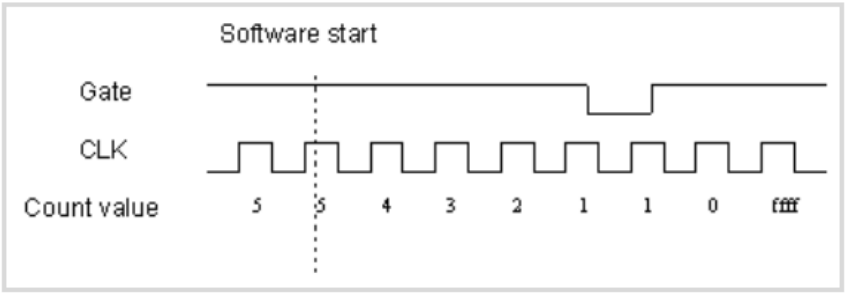


Figure 3-32: Simple Gated-Event Counting

Mode 2: Single Period Measurement

The counter counts the period of the signal on GPTC_GATE in terms of GPTC_CLK. The initial count can be loaded from software. After software-start, the counter counts the number of active edges on GPTC_CLK between two active edges of GPTC_GATE. After the completion of the period interval on GPTC_GATE, GPTC_OUT outputs high and then the current count value can be read back by software. Figure 3-33 illustrates the operation where initial count = 0, count-up mode.

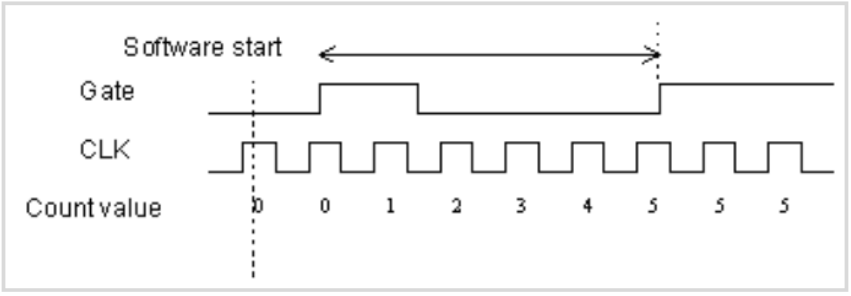


Figure 3-33: Simple Period Measurement

Mode 3: Single Pulse-width Measurement

The counter counts the pulse-width of the signal on GPTC_GATE in terms of GPTC_CLK. The initial count can be loaded from software. After software-start, the counter counts the number of active edges on GPTC_CLK when GPTC_GATE is in its active state. After the completion of the pulse-width interval on GPTC_GATE, GPTC_OUT outputs high and then the current count value can be read back by software. Figure 3-34 illustrates the operation where initial count = 0, count-up mode.

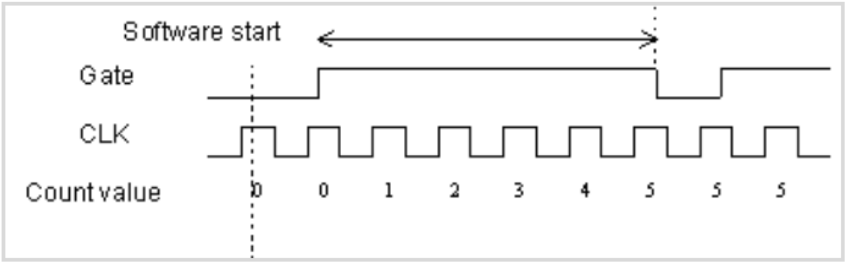


Figure 3-34: Simple Pulse-width Measurement

Mode 4: Single Gated Pulse Generation

This generates a single pulse with programmable delay and programmable pulse-width following software-start. The two programmable parameters can be specified in terms of periods of the GPTC_CLK input by software. GPTC_GATE is used to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 3-35 illustrates the generation of a single pulse with a pulse delay of two and a pulse-width of four.

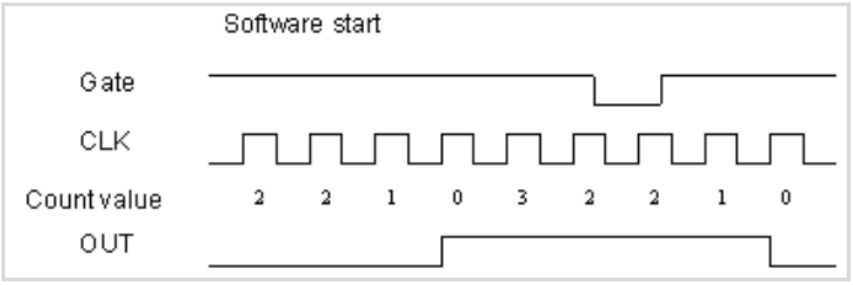


Figure 3-35: Simple Gated Pulse Generation

Mode 5: Single Triggered Pulse Generation

This mode generates a single pulse with programmable delay and programmable pulse-width following an active GPTC_GATE edge. You may specify these programmable parameters in terms of periods of the GPTC_CLK input. When the first GPTC_GATE edge triggers the single pulse, GPTC_GATE takes no effect until software-start is executed again. Figure 3-36 illustrates the generation of a single pulse with a pulse delay of two and a pulse-width of four.

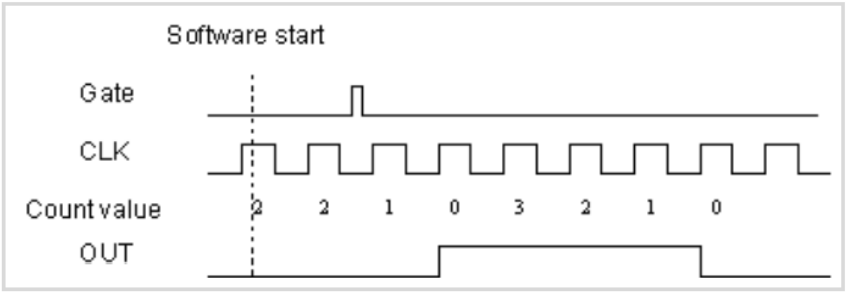


Figure 3-36: Simple Triggered Pulse Generation

Mode 6: Re-triggered Single Pulse Generation

This mode is similar to Mode 5 except that the counter generates a pulse following every active edge of GPTC_GATE. After software-start, every active GPTC_GATE edge triggers a single pulse with programmable delay and pulsewidth. Any GPTC_GATE triggers that occur when the prior pulse is not completed is ignored. Figure 3-37 illustrates the generation of two pulses with a pulse delay of two and a pulse width of four.

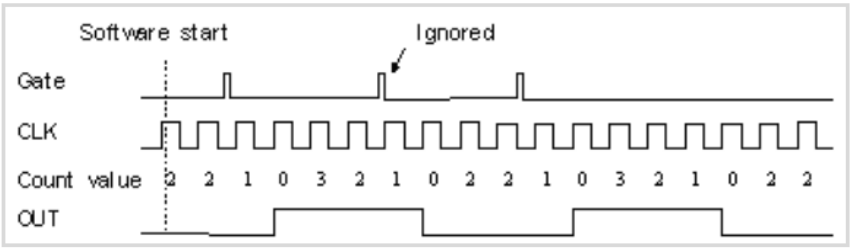


Figure 3-37: Re-triggered Single Pulse Generation

Mode 7: Single Triggered Continuous Pulse Generation

This mode is similar to Mode 5 except that the counter generates continuous periodic pulses with programmable pulse interval and pulse-width following the first active edge of GPTC_GATE. When the first GPTC_GATE edge triggers the counter, GPTC_GATE takes no effect until software-start is executed again. Figure 3-38 illustrates the generation of two pulses with a pulse delay of four and a pulse-width of three.

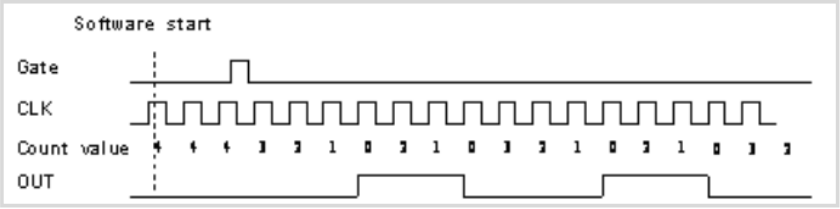


Figure 3-38: Re-triggered Single Pulse Generation

Mode 8: Continuous Gated Pulse Generation

This mode generates periodic pulses with a programmable pulse interval and pulse-width following software-start. GPTC_GATE is use to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 3-39 illustrates the generation of two pulses with a pulse delay of four and a pulse-width of three.

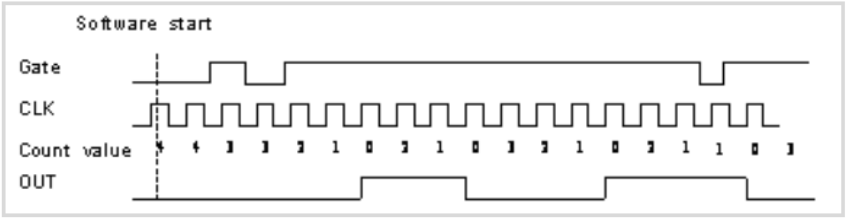


Figure 3-39: Continuous Gated Pulse Generation

3.5.3 PWM Modes

The PCIe-9100 Series powerful timer/counter can also simulate a PWM (Pulse Width Modulation) output. By setting varying number of Pulse_initial_cnt and Pulse_length_cnt, you can get a varying pulse frequency (Fpwm) and duty cycle (Dutypwm). This parameters can change immediately when PWM mode is operating COF (Change on the Fly). Figure 3-40 illustrates the PWM output and the formula showing how to calculate the PWM frequency and duty cycle.

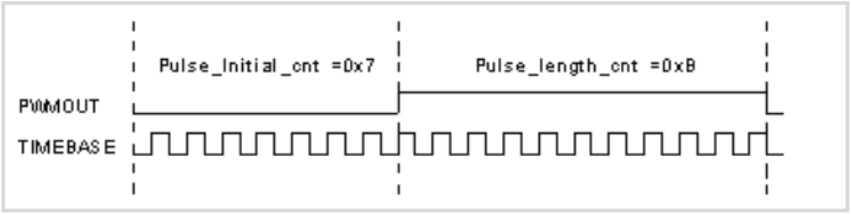


Figure 3-40: PWM Mode

$$F_{PWM} = \frac{F_{Timebase}}{Pulse_initial_cnt + Pulse_length_cnt}$$

$$Duty_{PWM} = \frac{Pulse_length_cnt}{Pulse_initial_cnt + Pulse_length_cnt}$$

3.6 Encoder

The PCIe-9100 Series features a simple motion control with support for two channel encoder input sets which provide an alternative for a step motor or servo motor's position feedback. The encoder sets are assigned in CN1 or CN8 depending on the model.

Definition	Pin No.		Definition
	1	35	
	…	…	
EA0+	17	51	EA0-
EB0+	18	52	EB0-
EZ0+	19	53	EZ0-
EORG0+	20	54	
	21	55	EORG1
EA1+	22	56	EA1-
EB1+	23	57	EB1-
EZ1+	24	58	EZ1-
DGND	25	59	
	26	60	
	27	61	
	28	62	
	29	63	
	30	64	
	31	65	
	32	66	
	33	67	
DGND	34	68	

Table 3-22: PCIe 9146/9147 CN1 Encoder Mode Pin Assignments

Definition	Pin No.		Definition
EA0+	1	2	EA0-
EB0+	3	4	EB0-
EZ0+	5	6	EZ0-
EA1+	7	8	EA1-
EB1+	9	10	EB1-
EZ0+	11	12	EZ1-
	13	14	
	...	...	
	17	18	DGND
	19	20	

Table 3-23: PCIe 9161/9163/9164 CN8 Encoder Mode Pin Assignments

Encoder Input Module

Figure 3-41 illustrates the encoder isolation phase A, phase B and phase Z inputs module.

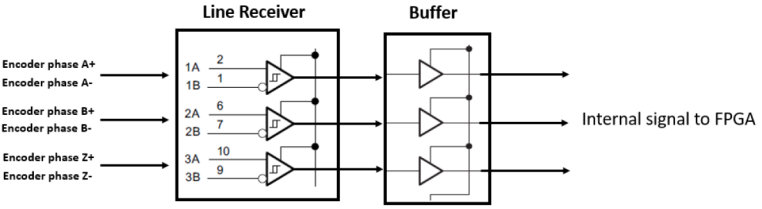


Figure 3-41: Encoder Input Module

The Encoder OGRx input is different from the encoder phase input since you need to add external +24V power to drive the photo-couple. Figure 3-42 shows the OGRx input.

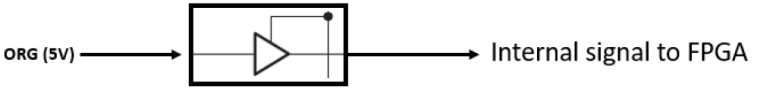


Figure 3-42: Encoder OGRx Input

CW/CCW Encoder Mode

When the Encoder is set to CW/CCW mode and when the input EAx is connected to a CW source signal and EBx is connected to a CCW source signal, pulses from EAx will cause the counter to count up and spin the motor clockwise.

Otherwise, pulses from EBx will cause the counter to count down and spin the motor counterclockwise. Figure 3-43 shows the increase/decrease of the counter value in CW or CCW encoder mode.

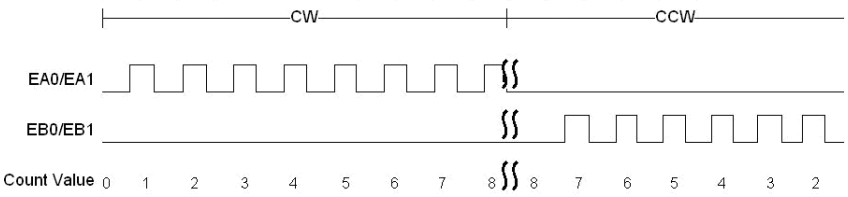


Figure 3-43: CW/CCW Encoder Timing

X1 Encoder Mode

In X1 encoder mode, if phase A (EA0/EA1) is ahead of phase B (EB0/EB1) in a quadrature cycle, the counter value will increase by 1. Otherwise, if phase B is ahead of phase A in a quadrature cycle, the counter value will decrease by1.

Figure 3-44 shows a quadrature cycle and the increase and decrease of counter value in X1 encoder mode. When phase A leads phase B, the counter value increases on the first rising edge of CLK after phase A goes high. When phase B leads phase A, the counter value decreases on the first rising edge of CLK after phase A goes low.

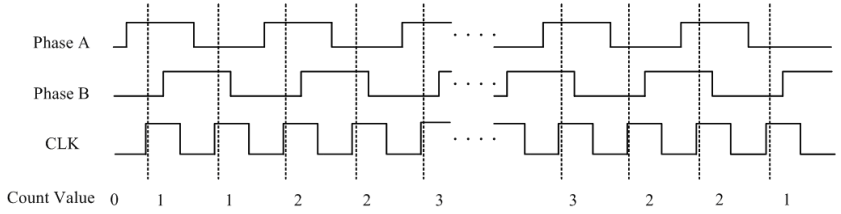


Figure 3-44: X1 Encoder Mode

X2 Encoder Mode

This mode is similar to X1 Encoder Mode, except that the amount of the counter value increases or decreases by two. Refer to Figure 3-45.

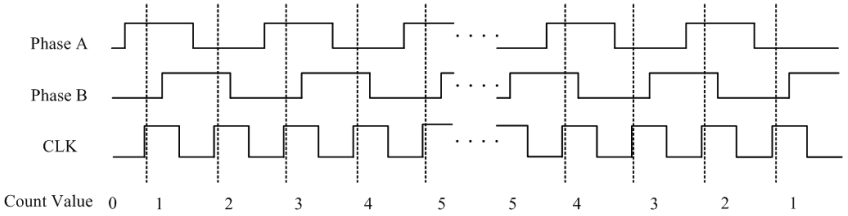


Figure 3-45: X2 Encoder Mode

X4 Encoder Mode

This mode is similar to X1 Encoder Mode, except that the amount of the counter value increases or decreases by four. Refer to Figure 3-46.

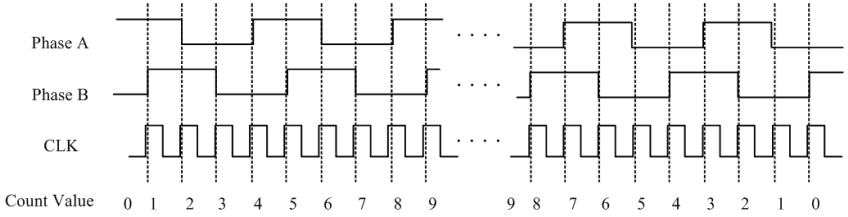


Figure 3-46: X4 Encoder Mode

Phase Z

Each encoder mode can use a third phase, phase Z, that is also frequently used for the index phase. You can decide if the counter needs to reload a specified value when phase Z is at a logic high level with phase A and B at a specific logic condition.

You must ensure that the logic level of phase Z is high during at least a portion of the phase you specify for reload when you use phase Z; otherwise, the counter does not reload.

In Figure 3-47, the reload phase is when the logic level of phase A is high, phase B is low, and phase Z is high in X1 Encoder Mode. In addition, reloading takes higher priority than inceasing or decreasing of the counter value. The reload occurs within one maximum CLK period after the reload phase becomes true. After the counter value is reloaded, the counter continues to count as before.

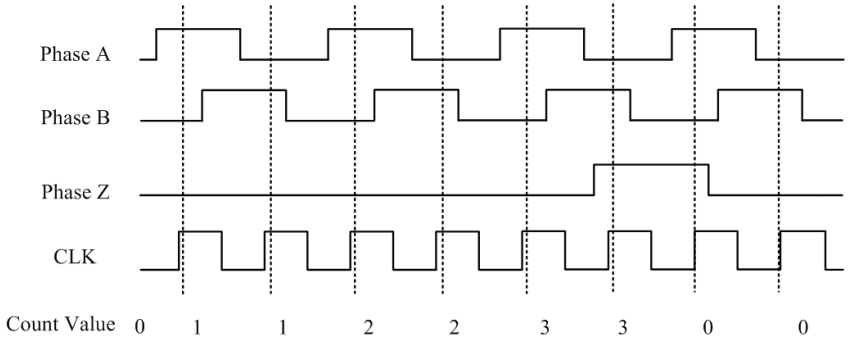


Figure 3-47: Phase Z

Original Signal (ORGx)

Original Signal (ORG0/ORG2/ORG1) is used with phase Z.

With ORG enabled, a high level on phase Z and ORG causes the counter to reload with a specified value in a specified phase of the quadrature cycle. When you use the ORG signal if it is at a low level and phase Z is at a high level, then the counter reload is ignored.

NOTE:

ORGx signal pin of PCIe-9146/9147 only support 5V TTL compatible signal.

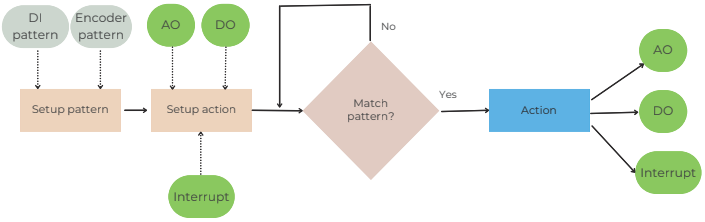
3.7 Pattern Match

The PCIe-9161/9163/9164 cards feature a pattern matching function, which automatically performs preassigned actions upon encountering predefined patterns without involving any software. With this pattern match function, users can achieve real-time process control for any aspect application.

The patterns predefined could be programmable DI codes on DI port or position values from the encoder interface. Up to 1024 sets of DI can be defined for each of encoder#0 and encoder#1.

Once set, whenever specific patterns are met, the PCIe-9161/9163/9164 will perform the preassigned actions on its AO port or DO port, with/without asserting corresponding interrupt event to the user's application.

The process flow of the pattern match function is outlined below..



The following is a list of the operational mode combinations that the pattern match function can perform.

- Interrupt-event
- Output DO status in static polling mode or DO pattern in continuous mode
- Output AO level in static polling mode or AO waveform in continuous mode
- Output DO status in static polling mode or DO pattern in continuous mode with applied interrupt-event
- Output AO level in static polling mode or AO waveform in continuous mode with applied interrupt-event

NOTE:

For detailed usage of the pattern match function, please refer to the example codes of PCIe-9161/9163/9164.

3.8 Programmable Function I/O

The PCIe-9146/9147/9161/9163/9164 supports a powerful programmable function I/O provided by an FPGA chip. These functional I/Os can be configured to three modes by software.

- Mode 0: TTL compatible Digital Input/Output (See “Digital Input and Output” on page 79.)
- Mode 1: 32-bit timer/counters (See “General Purpose Timer/Counter” on page 88.)
- Mode 2: Encoder input (See “Encoder” on page 99.)

Important Safety Instructions

For user safety, please read and follow all instructions, Warnings, Cautions, and Notes marked in this manual and on the associated device before handling/operating the device, to avoid injury or damage.

S'il vous plaît prêter attention stricte à tous les avertissements et mises en garde figurant sur l'appareil , pour éviter des blessures ou des dommages.

- Read these safety instructions carefully
- Keep the User's Manual for future reference
- Read the Specifications section of this manual for detailed information on the recommended operating environment
- The device can be operated at an ambient temperature of 50ºC
- When installing/mounting or uninstalling/removing device; or when removal of a chassis cover is required for user servicing:
  - Turn off power and unplug any power cords/cables
  - Reinstall all chassis covers before restoring power
- To avoid electrical shock and/or damage to device:
  - Keep device away from water or liquid sources
  - Keep device away from high heat or humidity
  - Keep device properly ventilated (do not block or cover ventilation openings)
  - Always use recommended voltage and power source settings
  - Always install and operate device near an easily accessible electrical outlet
  - Secure the power cord (do not place any object on/over the power cord)
  - Only install/attach and operate device on stable surfaces and/or recommended mountings
- If the device will not be used for long periods of time, turn off and unplug from its power source

- Never attempt to repair the device, which should only be serviced by qualified technical personnel using suitable tools
- A Lithium-type battery may be provided for uninterrupted backup or emergency power.

Risk of explosion if battery is replaced with one of an incorrect type; please dispose of used batteries appropriately.
Risque d'explosion si la pile est remplacée par une autre de type incorrect. Veuillez jeter les piles usagées de façon appropriée.

- The device must be serviced by authorized technicians when:
  - The power cord or plug is damaged
  - Liquid has entered the device interior
  - The device has been exposed to high humidity and/or moisture
  - The device is not functioning or does not function according to the User's Manual
  - The device has been dropped and/or damaged and/or shows obvious signs of breakage
- Disconnect the power supply cord before loosening the thumbscrews and always fasten the thumbscrews with a screwdriver before starting the system up
- It is recommended that the device be installed only in a server room or computer room where access is:
  - Restricted to qualified service personnel or users familiar with restrictions applied to the location, reasons therefor, and any precautions required
  - Only afforded by the use of a tool or lock and key, or other means of security, and controlled by the authority responsible for the location
- If PoE (Power over Ethernet) is enabled for the device, the system can ONLY be deployed indoors. Unless otherwise noted, the PoE system is NOT designed to withstand the rigors of outdoor use.

	BURN HAZARD Touching this surface could result in bodily injury. To reduce risk, allow the surface to cool before touching. ***RISQUE DE BRÛLURES*** *Ne touchez pas cette surface, cela pourrait entraîner des blessures.* *Pour éviter tout danger, laissez la surface refroidir avant de la toucher.*

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